SERVICE MANUAL

HIGH－RESOLUTION DISPLAY MONITOR

MODEL : HC3925 SERIES

MITSUBISHI ELECTRIC CORPORATION

NOV. 1991

X－RADIATION WARNING

The surface of picture tube may generate X-Radiation. Precaution during servicing, and if possible use of a lead apron or metal for shielding is recommended. To avoid possible exposure to X-Radiation and electrical shock hazard, the high voltage compartment and the picture tube shield must be kept in place whenever the chassis is in operation. When replacing picture tube use only designated replacement part since it is a critical component with regard to X-Radiation as noted above. The high-voltage specification is described on adjustment procedure.

CRITICAL COMPONENT REPLACEMENT WARNING

The components marked " ! " are critical components for X-Radiation. When replacing these parts, use exactly the same one. If broken the critical component, please contact with qualified personnel of Mitsubishi Electric Corp. or the company which indicated on name plate.

注 意

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CAUTION

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1991 JAN.
1991 MAR.11
1991 OCT. 7

TECHNICAL SPECIFICATION

FOR

19" V AUTO-TRACKING COLOR DISPLAY MONITOR

BASE MODEL NAME HC3925ATK

REVISED PAGES

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MITSUBISHI ELECTRIC CORPORATION

REVISE

BI	Add Signal Cable (FA-5)	OCT.7.'91

MODEL NAME TABLE

1) VERSIONS

1. HC3925ATK (SHORT PERSISTENCE PHOSPHER)
2. HC3925L9ATK (LONG PERSISTENCE PHOSPHER)
3. HC3925ETKL (SHORT PERSISTENCE PHOSPHER)
4. HC3925L9ETKL (LONG PERSISTENCE PHOSPHER)

2) GEOGRAPHICAL REGION

1. SAFTY / FUSE

MODEL	GEO GRAPHOCAL REGION	SAFETY	EMI	X-RAY	FUSE
HC3925ATK HC3925L9ATK	USA / CANADA	UL ,CSA	FCC-B ,DOC-B	DHHS,HWC	UL , CSA 3.5A 250V
HC3925ETKL HC3925L9ETKL	Europe / Australia / Asia	TUV	VDE-B	PTB	SEMKO 3.15A 250V

2. EMISSION

MODEL	GEO GRAPHOCAL REGION	EMI	X-RAY	Electromagnetic Emissior
HC3925ATK HC3925L9ATK	USA / CANADA	FCC-B ,DOC-B	DHHS,HWC	ELF / VLF Anti-Static : OPTION
HC3925ETKL HC3925L9ETKL	Europe / Australia / Asia	VDE-B	PTB	ELF / VLF Anti-Static is standard

TUV : EN60950 , VDE0805/05.90 ZH1/618
FCC : 47CFR Part15 Subpart B
DOC : SOR/88-475,CSA C108.8-M1983
VDE : DBP Vfg.1046/84,VDE 0871/06.78
PTB : RoV Vom 8.1 1987
UL : UL478 (UL1950)
CSA : CSA C22.2 NO.220
ELF : MPR-I
VLF : MPR-I

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1. Scope

This specification defines the design and performance of a high resolution 20"(19"V) color CRT display monitor.
The monitor provides both analog video input and TTL video input, and which automatically adjusts to graphics board scanning frequencies from 15.7KHz to 38.0KHz for horizontal frequency and from 45Hz to 90Hz for vertical frequency.

2. Regulations

Refer to MODEL NAME TABLE.

3. Electrical Specifications

3.1 CRT Description

(1) Size	: 20 inch diagonal (19"V)
(2) Deflection angle	: 90 degree diagonal
(3) Electron gun	: In-line type
(4) Focusing method	: Electrostatic
(5) Convergence method	: Magnetic
(6) Mask type	: Black matrix
(7) Trio spacing	: 0.31mm
(8) Array	: Dot trios
(9) Phosphor type	: P22 ,BL9
(10) Phosphor persistence	: P22 ; Short-PERSISTENCE (HC3925ATK,HC3925ETKL) : BL9 ; Long-PERSISTENCE (HC3925L9ATK,HC3925L9ETI
(11) Face plate	: Tinted glass (52%)
(12) Surface treatment	: A ; Non-glare (Silica coating) : E ; Non-glare with antistatic electric
(13) Implosion protection	: Banded with mounting lugs

3.2 Power Supply

(1) Voltage	: Automatically selectable between 100 ~ 120VAC (±10%) and 220 ~ 240VAC (±10%)
(2) Frequency	: 50/60Hz (±1Hz)
(3) Power consumption	: 140Watts (Max.)
(4) Inrush current	: less than 50A (0-peak)
(5) AC leakage current	: less than 750 μA (measured by IEC-950)

3.3 Signal Input

Refer Fig.5

3.4 Deflection

(1) Horizontal
Automatic synchronization : 15.7KHz ~ 38.0KHz

(2) Vertical
Automatic synchronization : 45Hz ~ 90Hz

3.5 High Voltage
High Voltage at CRT anode : 27.0KV±(typ) at 450μA

3.6 Degaussing

Manual degaussing : Activated at degauss sw on.

3.7 Color Control

3.7.1 Analog input

Unlimited

3.7.2 TTL input

The color control of TTL input provides Four (4) color modes which are 8 colors, saturated 16 colors, pastel 16 colors, and 64 colors, which is selectable by the color mode switch.

(1) 8 colors

INTENSITY	RED	GREEN	BLUE	COLOR
L	L	L	L	Black
L	L	L	H	Blue
L	L	H	L	Green
L	L	H	H	Cyan
L	H	L	L	Red
L	H	L	H	Magenta
L	H	H	L	Yellow
L	H	H	H	White

(2) Saturated 16 colors mode

INTENSITY	RED	GREEN	BLUE	COLOR
L	L	L	L	Black
L	L	L	H	Blue
L	L	H	L	Green
L	L	H	H	Cyan
L	H	L	L	Red
L	H	L	H	Magenta
L	H	H	L	Yellow
L	H	H	H	White
H	L	L	L	Gray
H	L	L	H	Light Blue
H	L	H	L	Light Green
H	L	H	H	Light Cyan
H	H	L	L	Light Red
H	H	L	H	Light Magenta
H	H	H	L	Light Yellow
H	H	H	H	Highlight White

(3) Pastel 16 colors mode

INTENSITY	RED	GREEN	BLUE	COLOR
L	L	L	L	Black
L	L	L	H	Blue
L	L	H	L	Green
L	L	H	H	Cyan
L	H	L	L	Red
L	H	L	H	Magenta
L	H	H	L	Brown
L	H	H	H	White
H	L	L	L	Gray
H	L	L	H	Pastel Blue
H	L	H	L	Pastel Green
H	L	H	H	Pastel Cyan
H	H	L	L	Pastel Red
H	H	L	H	Pastel Magenta
H	H	H	L	Pastel Yellow
H	H	H	H	Highlight White

(4) 64 colors (Example)

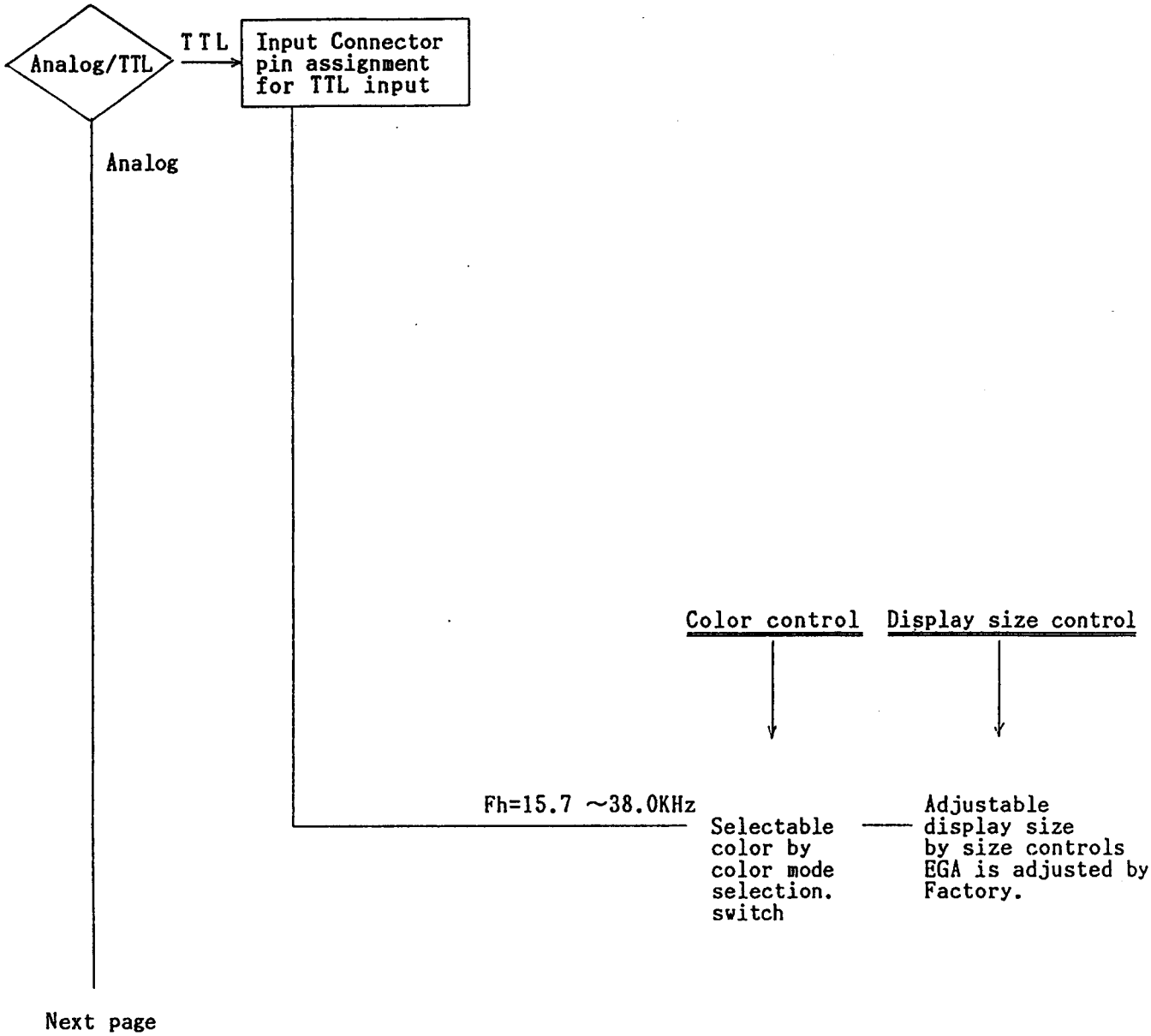
RED	red	GREEN	green	BLUE	blue	COLOR
H	H	H	H	H	H	Highlight White
H	L	H	L	H	L	White
L	H	L	H	L	H	Gray
L	L	L	L	L	L	Black
H	H	L	L	L	L	Light Red
H	L	L	L	L	L	Red
L	H	L	L	L	L	Dark Red
H	H	H	H	L	L	Light Yellow
H	L	H	L	L	L	Yellow
L	H	L	H	L	L	Dark Yellow
:		:		:		:
:		:		:		:

3.7.3 Text color

Displaying of only green,amber or white is selected by TEXT switch.
Note : The TEXT switch works only in the TTL mode.

3.8 MODE control

The monitor provides a input mode control which is to select a video signal-either TTL or ANALOG, and a AUTO mode control which is to be fully compatible with the IBM graphics adapter.



con't

Analog.

Input Connector
pin assignment
for analog input

Fh=15.7 ~38KHz

Display SIZE control

Adjustable
display SIZE
by size control
VGA,MACII , Super VGA
are adjusted by Factory .

4. Screen Characteristics

4.1 Test Conditions

Screen characteristics described in this section must be measured under any combination of the following conditions, unless otherwise specified.

(1) Operation mode	: VGA mode	
(2) Input power	: 120V AC 50Hz	
(3) Operating temperature	: 20±5 degree C	
(4) Magnetic field	: Horiz. 0.0 Gauss Vert. 0.4 Gauss 〈Northern Hemisphere〉	Horiz. 0.0 Gauss Vert. -0.4 Gauss 〈Southern Hemisphere〉
(5) Viewing direction	: Parallel to CRT axis	
(6) Brightness level	: (P22)90 cd/m^2 at white window. (BL9)50 cd/m^2 at white window.	
(7) Warm-up time	: 20 min.	

4.2 Luminance Range

	〈 P22 〉	〈 BL9 〉
Luminance control range	: from less than 20 cd/m^2 to more than 90 cd/m^2 measured at the center of white window.	from less than 20 cd/m^2 to more than 50 cd/m^2 measured at the center of white window.

4.3 Display Size : Horiz. 350mm±8mm
Vert. 265mm±8mm

4.4 Raster Regulation : less than 2% when CONTRAST control is adjusted over half range (ΔI_K 300 μA)

4.5 Display Centering : |g1-g2| ≦ 8mm
|g3-g4| ≦ 8mm
with reference to Fig.1.

4.6 Rotation : $\beta \leqq \pm 1$ deg.
with reference to Fig.1.

4.7 Geometric Distortion

(1) Trapezoid distortion : $\frac{AD-BC}{AD+BC} \times 100 \leqq 1.5\%$

: $\frac{AB-DC}{AB+DC} \times 100 \leqq 1.5\%$
with reference to Fig.1.

(2) Pincushion/Barrel distortion : $A \leqq 4.5$mm
$B \leqq 4.5$mm
with reference to Fig.2.

(3) Parallelogram distortion : $\alpha \leqq \pm 1$ deg.
with reference to Fig.2.

4.8 Linearity : Horiz. 7 % max.
Vert. 7 % max.
with reference to Fig.3.

4.9 Misconvergence : Center area within 0.3mm(typ.)
Circumference within 0.5mm.
The center area is defined as a center circule which diameter is equal to the vertical display size

4.10 White Color Specification

(1) Color Temperature (CIE chromaticity coordinates) : X=0.283 ±0.020=X(center)
Y=0.297 ±0.020=Y(center)
measured at the center of screen.

(2) Color Tracking Error : X=X(center)±0.020
Y=Y(center)±0.020
measured at the center of screen.

4.11 VIDEO BAND WIDTH
Dot clock rate : 50MHz(typ)

5. Mechanical Specifications

5.1 Enclosure (Refer to Fig.4)

(1) Dimension : Refer to OUT-LINE DRAWING

(2) Molded Material : ABS (94V-0)

(3) Color : Ivory white

(4) Texture : 30 μm.max.

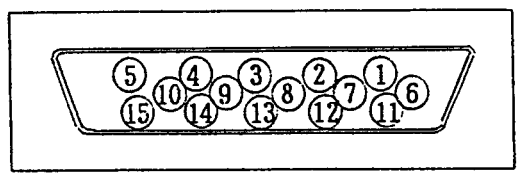
(5) TILT and SWIVEL base : Integrated with the Monitor Cabinet

5.2 Power Cord

2.5m cord and 3P plug

5.3 Signal Connector Pin Assignment

(1) D-Sub 15P shrinked connector
(Female)



Mounted on the rear panel

(2) Standard pin assignment for Signal-A

Pin Assignment \ Signal	TTL	ANALOG
1	———	RED GROUND
2	———	RED
3	———	GREEN GROUND
4	———	GREEN
5	———	BLUE GROUND
6	GROUND	GROUND
7	SECONDARY GREEN/INTENSITY	———
8	VERTICAL SYNC.	VERTICAL SYNC.
9	HORIZONTAL SYNC.	HORIZONTAL SYNC.
10	———	BLUE
11	GREEN	———
12	SECONDARY RED	———
13	RED	———
14	BLUE	———
15	SECONDARY BLUE	———

(3) Standard pin assignment for Signal-B

Pin Assignment \ Signal	ANALOG	CONTROL
1	RED GROUND	
2	RED	
3	GREEN GROUND	
4	GREEN	
5	BLUE GROUND	
6	GROUND	
7		
8	VERTICAL SYNC.	
9	HORIZONTAL SYNC.	
10	BLUE	
11		GROUND
12		REMOTE
13		R SIG B
14		R SIG A - A/T
15		

5.4 User Controls

(1) Front control

Power ON/OFF
Degauss SW.
Brightness
Contrast
V-SIZE
V-POSI
H-SIZE
H-PHASE

(2) Rear panel

TTL COLOR mode Switch
Color mode select switch

6. Environmental Conditions

6.1 Temperature and Humidity

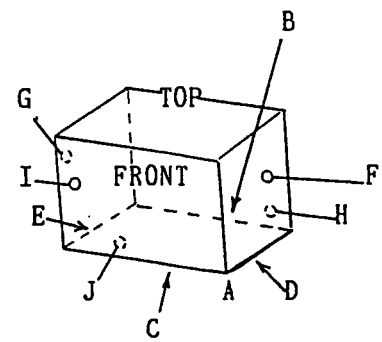
(1) Operating conditions : 0～40℃
10%～95%RH
without condensation

(2) Non-operating conditions : -10～55℃
5%～95%RH
without condensation

6.2 Altitude : 0～7000 feet at 40℃

6.3 Drop test

The inside unit shall be withstand without any damage by following procedure.
: Drop to the hard floor from the position of the followings,
corner(A),edge(B,C,D,E)and each surface (F,G,H,I,J)



Drop-height : 16" ··· B,C,D,E,J
12" ··· A,F,G,H,I

6.4 Vibration test

The inside unit shall be withstand without any damages by following test.
The packed unit is free on the vibration table.

: Freq.	11～33 Hz
: Amplitude	1.5 mm_{P-P}
: Sweep time	1 min
: Waveform	sinusoidal wave
: Direction	up/down
: Time	one hour

7. Factory Set Up

1) Switches

SIGNAL SELECT	SW	: SIGNAL-A ANALOG
TEXT	SW	: COLOR
Color Matrix	SW	: 8 colors,16 colos,64 colors

2) Accessories

Power cord

Signal Cable. (FA-5) B1

APPENDIX

Fig.1 Display Centering/Rotation and Trapezoid Distortion

Fig.2 Pincushion/Barrel and Parallelogram Distortion

Fig.3 Linearity

Fig.4 Enclosure Outline on HC3925ATK : DRAWING NO.

Fig.5 Schematic diagram of input circuit

Fig.1 Display Centering / Rotation and Trapezoid Distortion

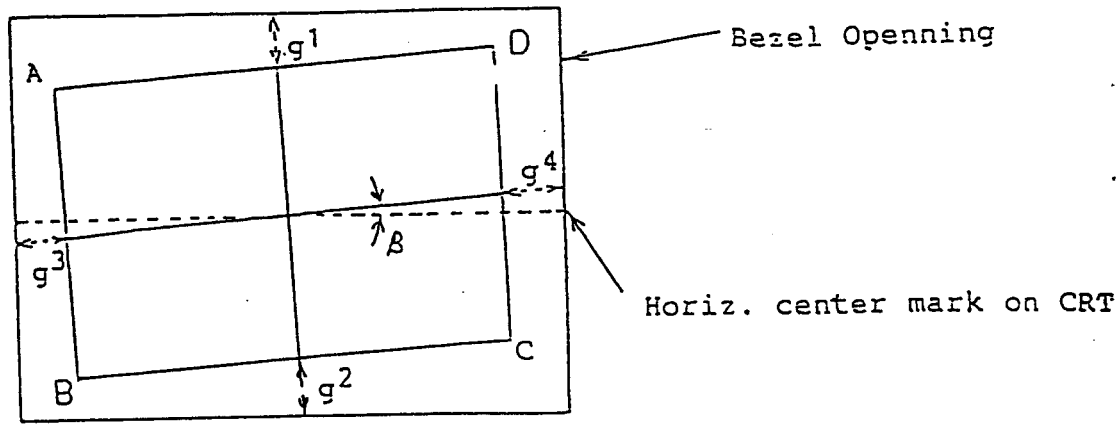


Fig.2 Pincushion / Barrel and Parallelogram Distortion

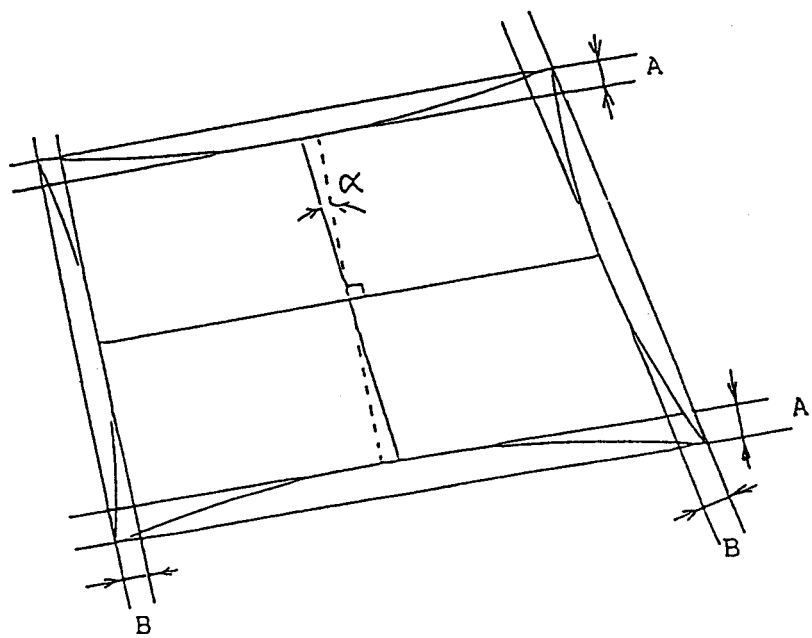
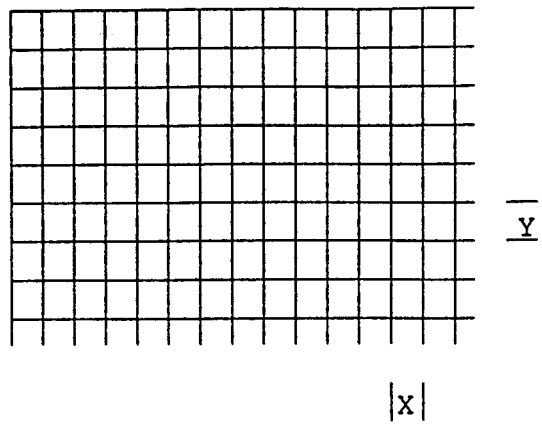


Fig.3 Linearity

Scanning nonlinearity is defined in terms of the pattern of horizontal (16 lines) and vertical (12 lines) lines produced by the cross-hatch pattern generator.

ex)



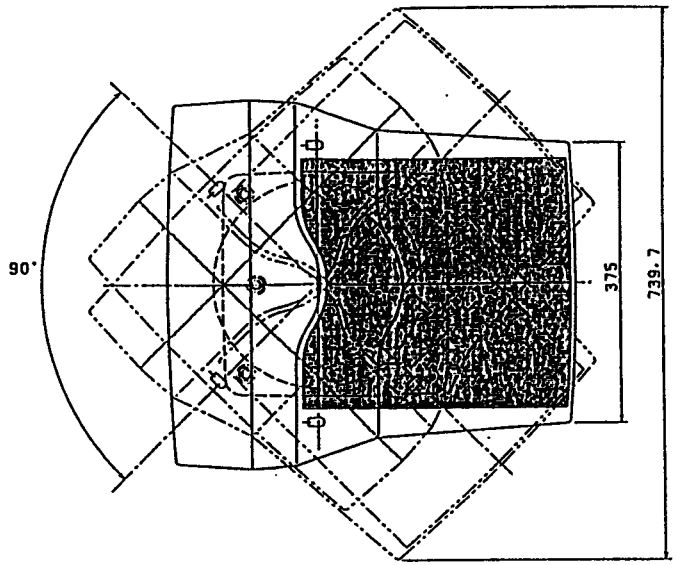
Horizontal nonlinearity

$$\frac{(X_{max}-X_{min})/2}{\overline{X}} \times 100 \quad (\%)$$

Vertical nonlinearity

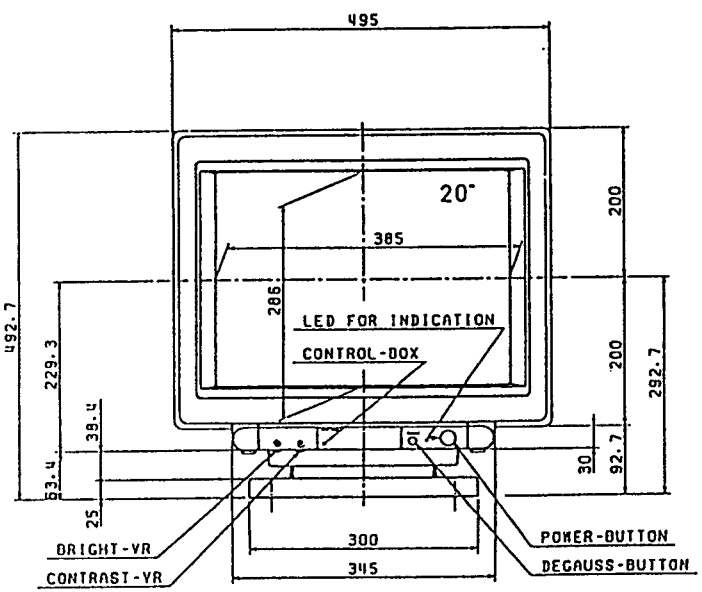
$$\frac{(Y_{max}-Y_{min})/2}{\overline{Y}} \times 100 \quad (\%)$$

TOP-VIEW

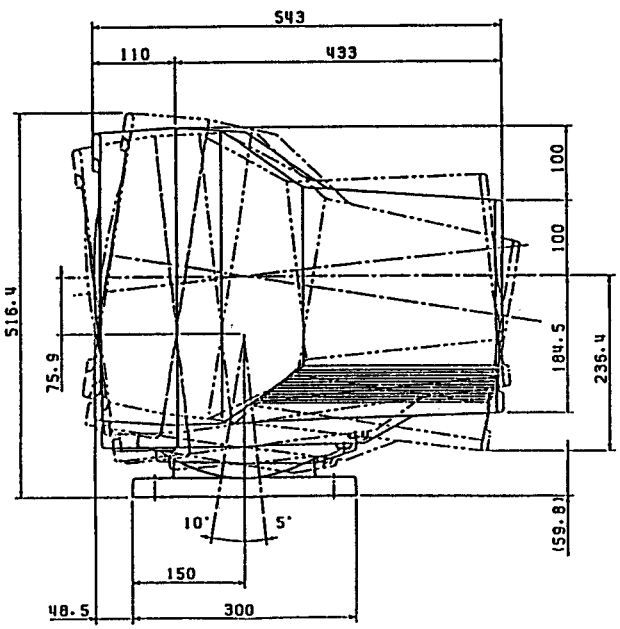


1. WEIGHT---APPROX 33.5KG
2. COLOR----GRAYISH WHITE

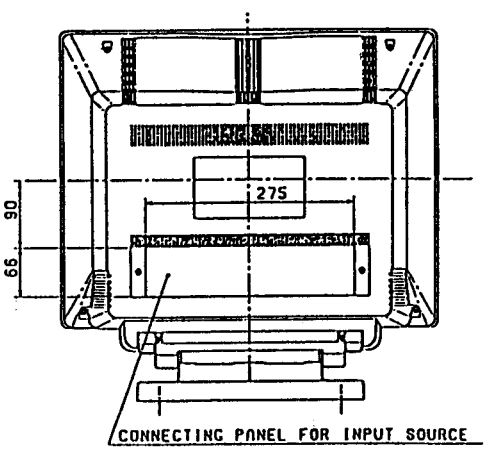
FRONT-VIEW



SIDE-VIEW



REAR-VIEW



20

CHANGE					CAD
				NEA 20C MONITOR WITH T/S STAND	
	MITSUBISHI ELECTRIC CORPORATION NAGASAKI WORKS				
	DRAWN		APPROVED	OUTLINE	
	CHECKED				
	DESIGNED				

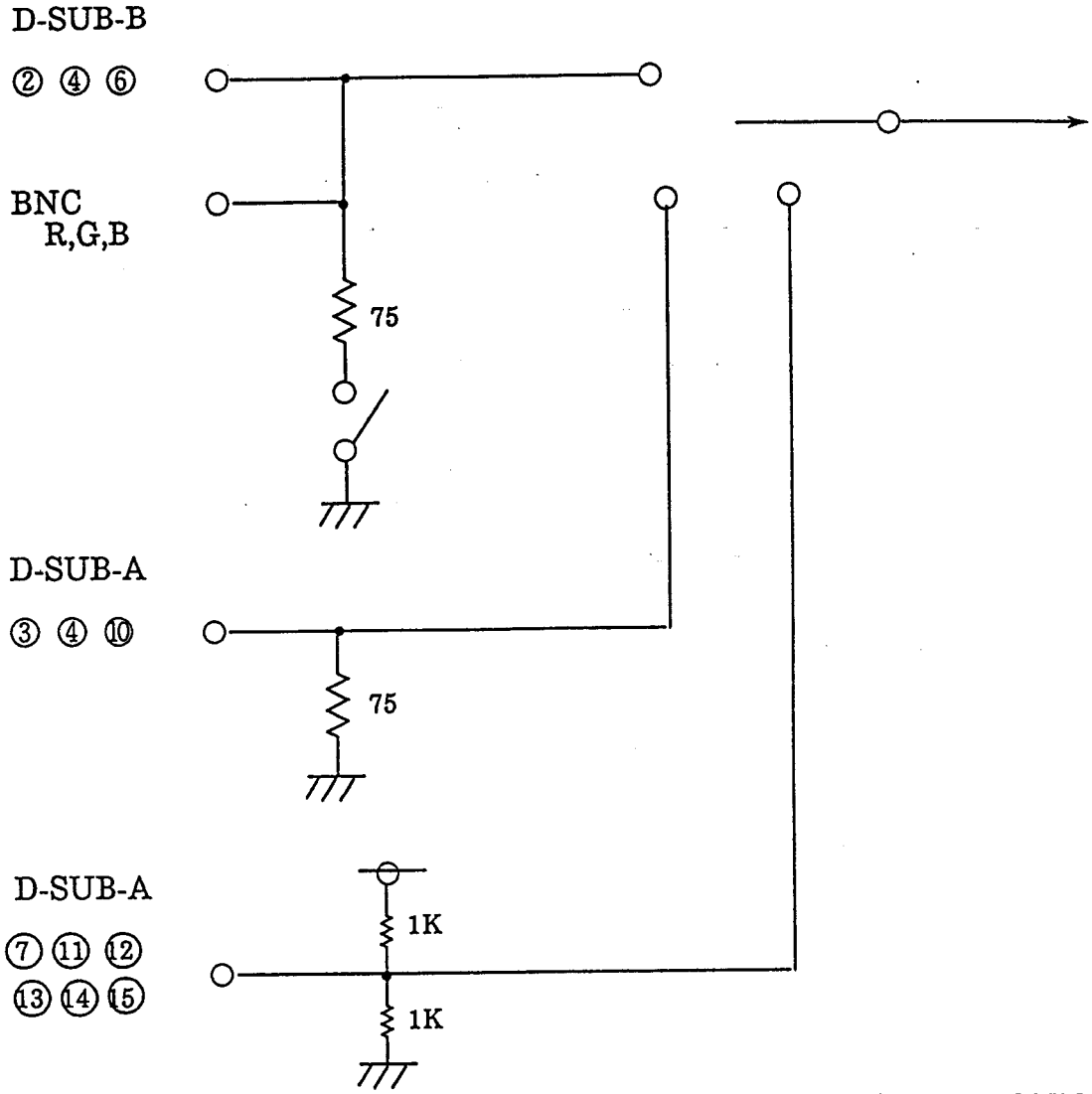


Fig. 5-1 Schematic Diagram of Video Input Circut.

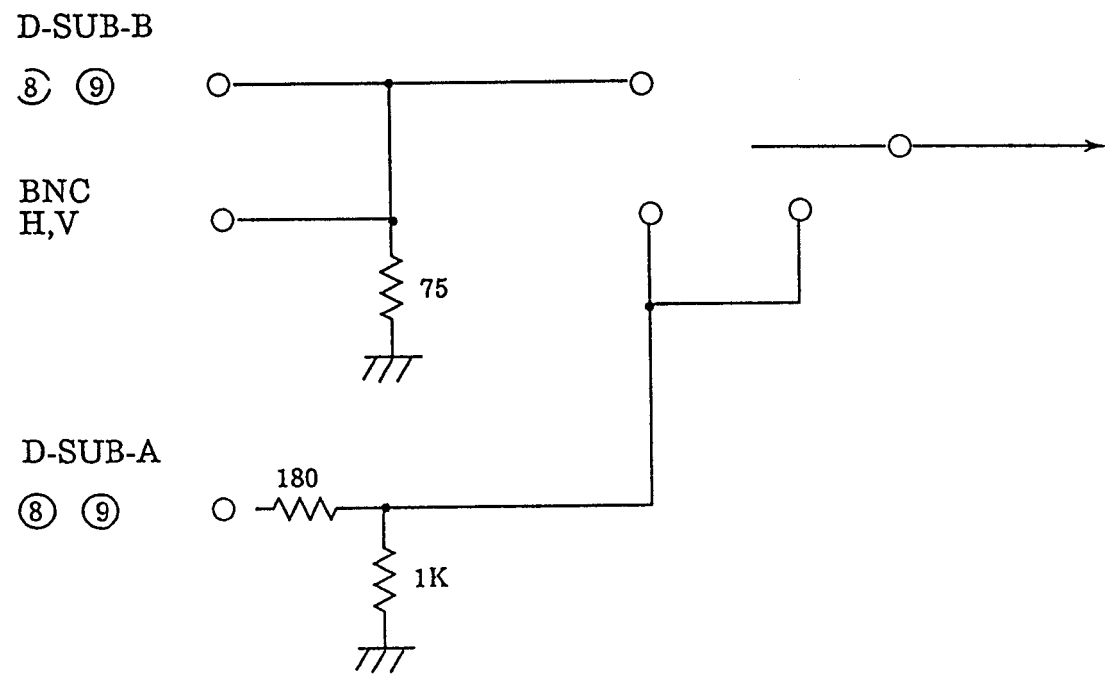


Fig. 5-2 Schematic Diagram of Sync Input Circut.

2. CIRCUIT DESCRIPTION

2.1 POWER SUPPLY BLOCK

2.1.1 GENERAL

(1) The power supply block can be operated in case either AC100~120V or AC200~240V power line.

(2) The selection of power line voltage is performed automatically.

(3) The output lines of this power supply are shown is TABLE 2－1 with thier main loads.

(4) The power supply works as switched mode opration with RCC (Ringing Choke Converter) configuration. Output voltages are regulated by 3rd winding. The switching frequency is corresponding to load currents.

The 45~110V line is regulated by the DC chopper method from 135V line.

VOLTAGE LINE	ACTUAL OUTPUT VOLTAGE	MAIN LOAD
135V	135V	HIGH VOLTAGE POWER SUPPPLY
+B	45~110V	HORIZONTAL DEFLECTION POWER SUPPLY
80V	80V	VIDEO AMPLIFIER CIRCUIT
28V	28V	VERTICAL DEFLECTION CIRCUIT
24V	24V	HORIZONTAL TRAKING CIRCUIT
12V	12V	VIDEO AMP, VERTICAL TRAKING CIRCUIT
5V	5V	CONTROL WITH MPU/GATE ARRAY
-6.3V	-6.3V	CRT HEATER

TABLE 2－1

2.1.2 RECTIFY AND FILTER CIRCUIT

(1) The AC input voltage is rectified by the diode bridge D901. The rectified voltage is filtered by charging C901 and C902.

(2) In case of AC100~120V line input, the rectify circuit works as double voltage rectifier circuit controld by IC901.

In case of AC200~240V line input, the rectify circuit works as a normal full wave rectifier circuit controlled by IC901.

(3) The thermistor TH901 is equipped to suppress the inrush current when powerswitch is turned on. The triac Q905 shunts TH901 to eliminate the power loss of TH901 after the control circuit starts to oscillate.

2.1.3 DEGAUSS CIRCUIT

This monitor is equipped the manual degauss function. When degauss switch is turned on, the relay RY901 work to operate the degaussing circuit.

The posistor RP901 and RP902 are selected by RY901 according to AC input voltage. The relay RY901 is switched automatically by IC901 depending on AC input voltage. Then degauss circuit works correctly both AC100~120V and AC200~240V.

2.1.4 PRIMARY CIRCUIT

(1) Main DC power supply of this monitor consists of RCC (Ringing Choke Converter). When the power SW is turned on, triggering current is fed through R905 and R909 to the 3pin of IC991 to flow the collector current of Q1 in IC991. The collector current of Q1 begins to flow, then inductive voltage is generated between 8 and 6pin of T931 so that the differential base current caused by C908 and R904 gives to the base of Q1. As the load current of secondary winding at power switched on, are very small, very small peak collector current I_P' of Q1 is needed. The circuit comes to stabilize by repeating the action stated above.

(2) In normal operating condition, the circuit works as follows.

The collector current I_C of Q1 increases according to the equation of

$$I_C = \frac{V_I}{L_P} T_{ON.}$$

(L_P:Primary winding inductance V_I:Input voltage)

When the I_C reaches $I_P = I_B \times hfe$, V_{CE} of Q1 increase immediately and the charge current for C922 flows through D1 and D909. In the same time secondary current begin to flow through D951~D955. As soon as the energy which is stored in primary winding of T931 transfers to secondary circuit, the current through D951~D955 also reach to 0 (zero). In that time all winding voltages of T931 are zero, and the Q1 strats. The base current of Q1 is supplyed from the charge of C922 by Q2 turned on.

(3) The third winding 7 −6pin of T931 works as the detector to stabilize the secondary voltage. If the voltage of secondary widings increase, voltage of 7 − 6pin also increase. So the rectified voltage which is supplied to 9pin of IC991

increases to by −pass the base current of Q1 through Q5, Q3. In that result, output voltage decrease.

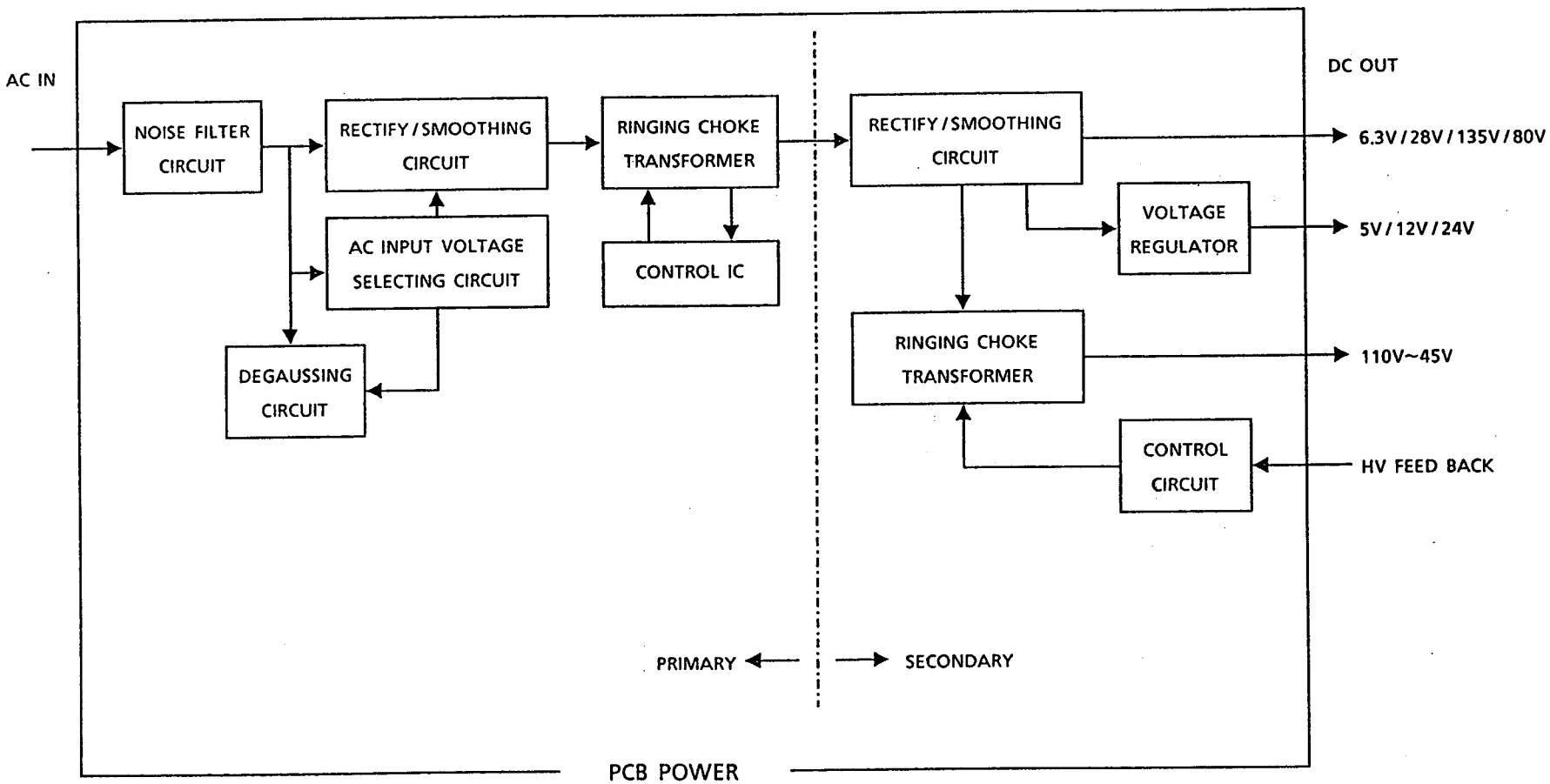
(4) D914 and D915 work as the protector for excess AC voltage. If the IC901 is broken in condition of continuing double voltage rectifier circuit and the Ac input is connected to 200V line, then avalance diode D914 and D915 will be turned to short the circuit. So the fuse F901 will be belowed, and components are avoided to be broken.

2.1.5 SECONDARY CIRCUIT

(1) In this paragraph, chopper circuit which is applied for auto−tracking circuit will be explained.

(2) Chopper circuit mainly consists of T951, Q951, Q952, Q953. During the Q951 is turned on, base current of Q951 is supplied by the discharge current from C969. When I_C of Q951 reaches to the saturated level $I_P = I_B \times hfe$, Q951 is turned off immediately. Then the voltage 6pin of T951 increase to charge the C969 through D958 to prepare the next switching cycle. The output voltage +B (Q951 emitter voltage) is regulated by following procedure. If the voltage of F/B terminal is higher, base current of Q953 increase. So the base current of Q952 also increase to by −pass the base current of Q951. In that result, peak collector current I_P of Q951 decreases to lower the output voltage.

FIG. 2-1 BLOCK DIAGRAM OF POWER SUPPLY CIRCUIT



2.2 DEFLECTION BLOCK

Deflection block consists of horizontal, vertical and high voltage circuits, and are fundamentatlly operated by changing DC control voltages.

2.2.1 HORIZONTAL DEFLECTION CIRCUIT

(1) All DC control voltages are fed from IC104, IC105 which are located on PCB — TERMINAL. Negative H — sync. signal is fed through 10pin of connector D1 from PCB — TERMINAL. If H — oscillation frequency is higher, relative DC voltage of 7pin of IC502 is lower, then charge current to add to time constant circuit consist of R520 increases to shorten charge time. So the oscillation frequency goes to higher, when no sync. signal is connected, free running frequency is approx. 25KHz.

(2) The output of 13pin of IC501 works as a drive voltage for H — deflection, and HV circuits. The principle of horizontal deflection is shown in FIG. 2 — 2. The voltage in FIG. 2 — 2 indicate approx. value at 38KHz operation. Q591 works as a horizontal output, and D591 and D545 work as dumper diodes. Q531, Q532, Q533, Q534 and RY501 are switched on as follows in accordance with the horizontal frequency to compensate the horizontal linearity.

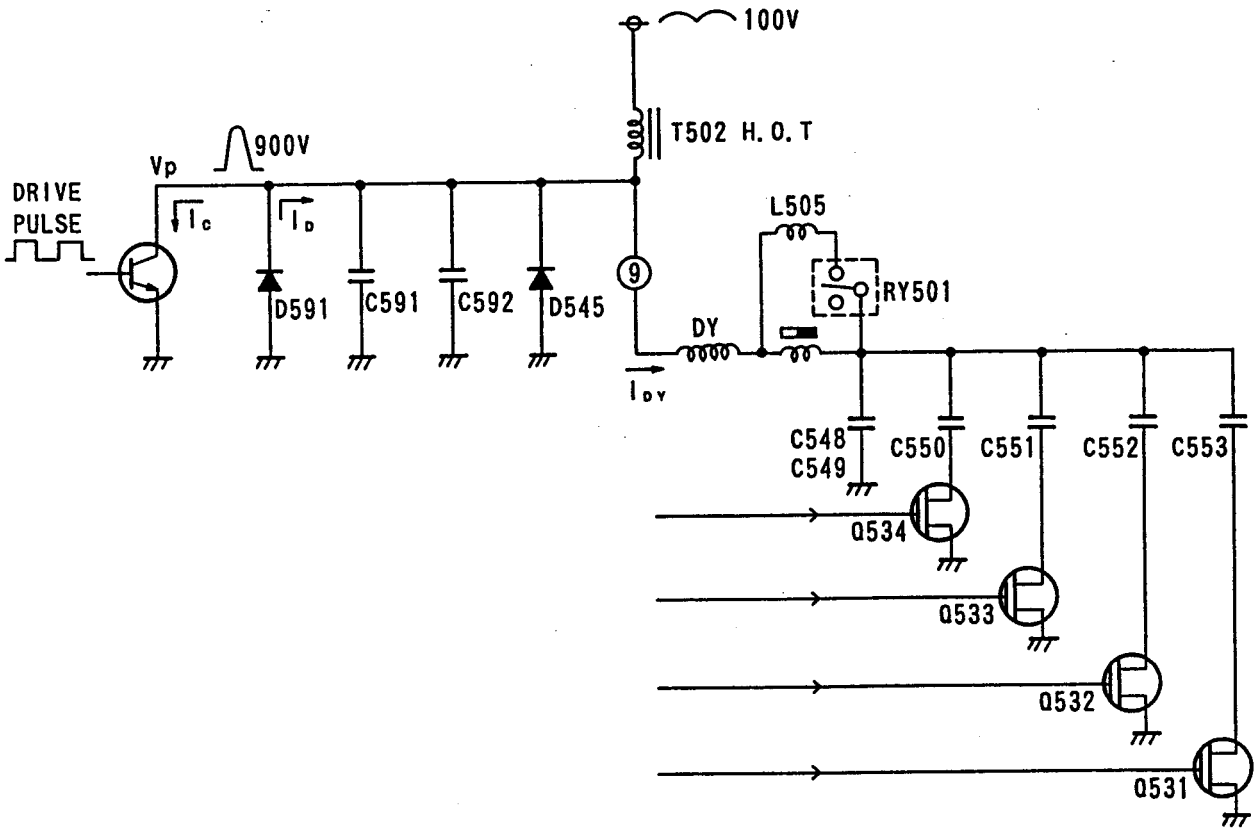
(3) In FIG. 2 — 2, the horizontal output transistor Q591 is turned on by the drive pulse from IC501 via Q505 and Q506. During Q591 is turned on, the deflection current I_{DY} increase from 0 to positive max. I_P in accordance with the equation $I_F = V_{CC} \times T_{ON} / L_{DY}$, ($L_{DY}$:Parallel value of hot and DY)

When the drive pulse goes to negative polarity, Q591 is turned off, and I_{DY} begins to flow to charge C591 and C592 until V_{CP} reaches maximum value $3.14 \times T_S \times V_{CC} / (2 \times Tr)$ as soon as V_{CP} reaches maximum value, discharge current from C591 and C592 flow to deflection yoke. This charge and discharge period is called "RETRACE TIME" which is expressed by equation

$$Tr = 3.14 \sqrt{L_{DY} \times C_r}$$

When the V_{CF} reached to 0V, the dumper diodes are turned on and I_{DY} begins to flow from $-I_P$ to 0ampere. The horizontal output transformer T502 works as a choke coil connecting between deflection yoke and power supply, and also works to get some DC power sources.

(4) The power supply voltage connected to 7pin of T502 is modulated to parabolic wave from by Q511 and Q593 to compensate side pin cushion distortion. The parabolic wave is generated and amplified by PCB — PCC and fed through buffer amplifier Q510 to modulate. Also 7pin of T502 voltage is varied from about 45V to 110V to regulate the horizontal width regardless of horizontal frequency. This is performed to maintain the DC voltage of the cathode of D505 which is



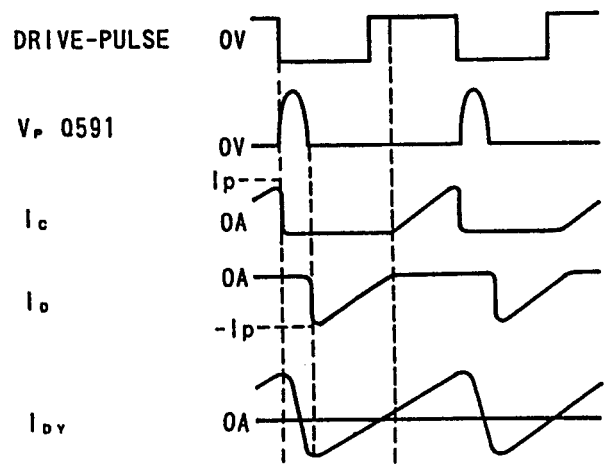


FIG. 2—2 PRINCIPLE OF HORIZONTAL DEFLECTION

proportional to collector voltage of Q591. If DC voltage across C542 is higher 12pin voltage of connector D5 also increases. So the +B voltage of 1pin of D5 becomes lower in procedure stated in 2.1.5 (2). (see attached FIG. 2−4)

(5) Q508 and Q592 consist of regulator to optimize condition of H −deflection output transistor Q591. Output voltage of Q592 is controlled by 2modes.

(5−1) If horizontal width is to wider, the H−DRIVE control voltage from 13 pin of IC505 increases, emitter current of Q508 decreases, then output voltage of Q592 increases to supply enough driving power for Q591.
Refer to FIG. 2−3.

(5−2) On the other hand, when the 13pin voltage of IC505 decreases according to the lower horizontal frequency, base voltage of Q508 also decreases, so the output voltage of Q592 increase to optimize the base current of Q591. Reffer to FIG. 2−4.

By the manner stated (5 − 1) and (5 − 2), Q591 is driven enough, and power loss minimized.

FIG. 2−3

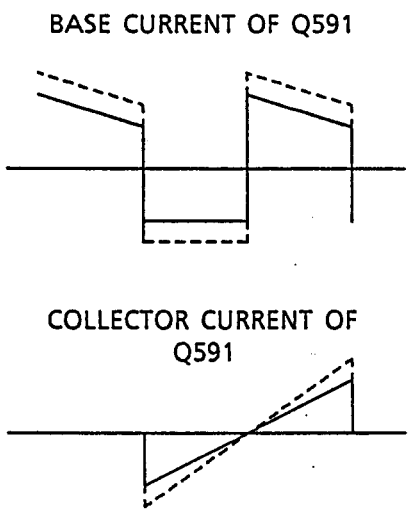
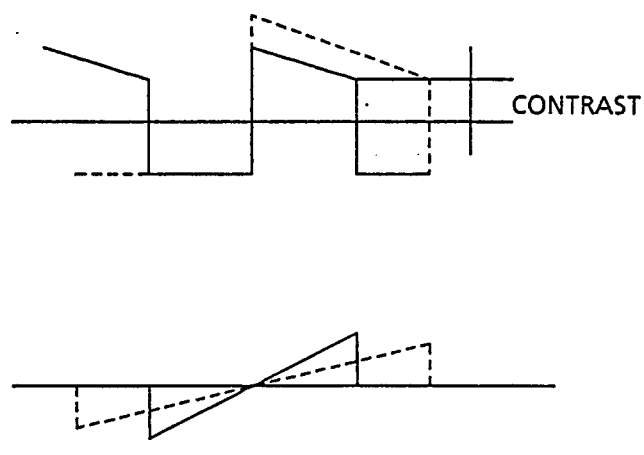


FIG. 2−4



(6) 1, 3pin of connector D2 are control signals to change AFC component C525~C528 and R516~R519. Combination of these are as follows.
See TABLE 2−2.

TABLE 2-2 SWITCHED COMPONENTS VS HORIZONTAL FREQUENCY

fh (KHz)	HORIZONTAL LINEARITY					RESONANE CAPACITOR OF HIGH VOLTAGE CIRCUIT			HORIZONTAL AFC				DRIVE
	C550	C551	C552	C553	L505	C576	C574	C573	C527 R519	C528 R517	C526 R516	C525 R518	IC505 13pin (V)
15	ON	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	OFF	OFF	0
16	ON	ON	ON	ON	OFF	ON	ON	ON	ON	OFF	OFF	OFF	0.3
17	ON	ON	OFF	ON	OFF	ON	ON	ON	ON	OFF	OFF	OFF	0.7
18	ON	ON	OFF	ON	OFF	ON	ON	ON	ON	OFF	OFF	OFF	1.1
19	ON	ON	OFF	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	1.5
20	ON	OFF	ON	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	1.8
21	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	2.2
22	ON	OFF	OFF	ON	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	2.6
23	ON	OFF	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	OFF	OFF	3.0
24	OFF	ON	ON	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	3.3
25	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	3.7
26	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	OFF	OFF	4.1
27	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	4.5
28	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	4.8
29	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	5.2
30	OFF	OFF	ON	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	5.6
31	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	6.0
32	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	6.3
33	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	6.7
34	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF	7.1
35	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	7.5
36	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	7.8
37	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	8.2
38	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	8.6

2.2.2 HIGH VOLTAGE CIRCUIT

(1) HIGH VOLTAGE SUPPLY AND CONTROL CIRCUIT

The principle of the high voltage supply circuit is basically same as the horizontal deflection.

The drive pulse which is same as the horizontal deflection is connected to base of Q594 via Q517 and switches Q594. The flyback transformer steps up collector pulse generated when Q594 turned off to the high voltage. The high voltage should be stabilized to prevent the fluctuation of the size of the image on screen regardless of the beam current. In this circuit, the supply voltage is contolled to stabilize the high voltage output. The series regulator composed of Q595 and Q519 controlls the supply voltage of the circuit. The high voltage is attenuated by the high voltage resistor, approx. 800mega ohms, equipped inside the flyback transformer, and R5B6. This voltage is fed to the base of Q519 which works as the error amplifier for the series regulator via the emitter follower Q521, and is compared with reference voltage stabilized by D524. If the high voltage increases, the feed back voltage also increases, and the base current of Q519 increases and the collector voltage of Q519 decreases, and then the emitter voltage of Q595 decreases. It means the decrease of the supply voltage to the high voltage circuit, and the initial increase of the high voltage is corrected.

Q535, Q536 and Q537 are switched on as follows in accordance with the horizontal frequency to change the total value of the resonance capacitor C586, C587 and C588. (see attached TABLE 2−2)

The high voltage is set to the pre−arranged value (27KV STD.) by VR503 (HV−ADJ).

(2) HIGH VOLTAGE SAFETY CIRCUIT

> CAUTION
> Safety circuit described below are equipped to prevent abnormal increase of the high voltage that may cause a X−Radiation of harmful level.
> No modification should be applied to the high voltage supply and safety circuit.

The safety circuit works as the over voltage protector for high voltage. The high voltage is attenuated by the high voltage resistor, approx. 550mega ohms, equipped inside the flyback transformer, and R5C1. This voltage is fed to the base of Q522 which works as the emitter follower and used as the high voltage detecting. The voltage of anode of D525 is adjusted to the triggering voltage level just in case of the high voltage reaches 30KV, by VR504 (HV−PRO). When

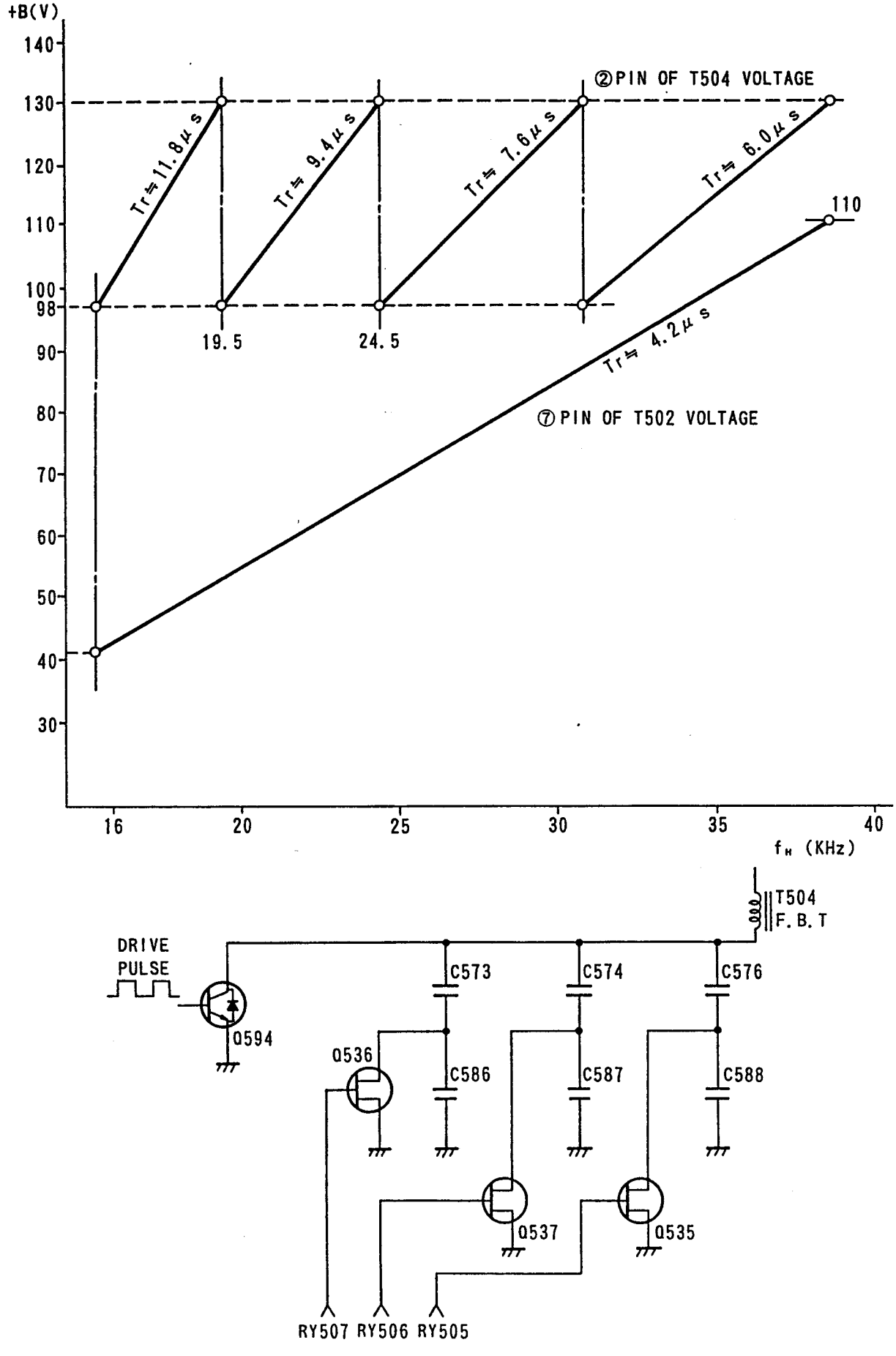


FIG. 2—5 SUPPLY VOLTAGES TO T502, T504 VS HORIZONTAL FREQ.

the high voltage reaches 30KV under some trouble conditions, X－Ray protection component Q518 works to inhibit drive pulse from IC501. So no switching operation which generates high voltage works. As Q518 is thyristor, it continues to 0 (zero) until the power swtich is turned off by the operater.

2.2.3 VERTICAL DEFLECTION CIRCUIT

Vertical deflection is performed by one IC, and some attached components.

(1) The oscillating frequency is controlled by applying DC voltage at 4pin of IC401 via 5pin of IC505. If the DC voltage at 4pin of IC401 is higher and threshhold level goes to high, oscillating frequency goes to lower.

(2) 3pin of IC505 works as height controller to be changed the DC voltage. When DC voltage is lower, vertical height becomes to wider.

2.3 VIDEO

2.3.1 GENERAL

(1) The monitor can be input the following signals.

(1)−1 Separated Analog video + Separated TTL sync.

(1)−2 Separated Analog video + Separated Analog sync.

(1)−3 Separated Analog video + Separated TTL sync.

(1)−4 Separated Analog video + Composite Analog sync.

(1)−5 Sync. on Green

(1)−6 Separated TTL video + Separated TTL sync.

(1)−7 Separated TTL video + Composite TTL sync.

The TTL and Analog sync. signal are available to both polarity (negative or positive).

(2) Selection of input signal

This monitor has 3 different video signals applied to the shrinked D −sub 15pin or BNC on the rear panel.

Signal−A (shrinked D−sub 15pin)	Analog, TTL video input
Signal−B (BNC)	Analog video input
Signal−B (shrinked D−sub 15pin)	Analog video input
	REMOTE CONTROL signal

And these signals are selected by SIGNAL INPUT SELECT SWITCH on the front control panel or REMOTE CONTROL signal from computer provide to the rear shrinked D−sub15 pin of Signal−B.

PIN NO. 12	PIN NO. 13	PIN NO. 14	REMARK
REMORT = HIGH (OPEN)	DO NOT CARE	DO NOT CARE	Selected by SIGNAL INPUT SELECT SWITCH
REMORT = LOW	HIGH	DO NOT CARE	Signal−B select
	LOW	HIGH	Signal−A (Analog) select
	LOW	LOW	Signal−A (TTL) select

TABLE 2−3 REMOTE CONTROL SIGNAL INPUT

(3) TTL input

The TTL input signal is converted to digital to analog signal by IC101 which output is selectable to 8 or pastel 16 or saturated 16 or 64colors by COLOR MODE SELECT SWITCH on the rear panel. This monitor has TEXT display which display white, green or amber monochrome color. (only at TTL input)

(4) Analog input

The Analog input signal or digital to analog converted TTL signal is applied to preamplifier IC201 which also controls the DC clamping level, bias and gain. The DC clamping is determined by clamp pulse of 15pin and clamp level voltage of 16pin on IC201. The gain is determined by DC voltage of 14pin on IC201. Each gain of R, G or B is determined by DC voltage of 4pin, 8pin or 12pin on IC201.

(5) BRIGHTNESS, CONTRAST controls

The BRIGHTNESS control is equipped to control bias level and the CONTRAST control is equipped to control 3video gains.

2.3.2 VIDEO CIRCUIT

This monitor has 3different video signals applied to the shrinked D−sub 15pin or BNC. These signals are selected are selected by SIGNAL INPUT SELECT SWITCH or REMOTE CONTROL SIGNAL from computer provide to the rear shrinked 15pin of Signal−B applied to signal selection circuit. The signal selection circuit is consist of Q1A2, Q1C2, Q1D2 and IC105. One of the selected video signal by signal selection circuit is applied to pre−amplifier IC201.

(1) BLOCK DIAGRAM OF VIDEO CIRCUIT

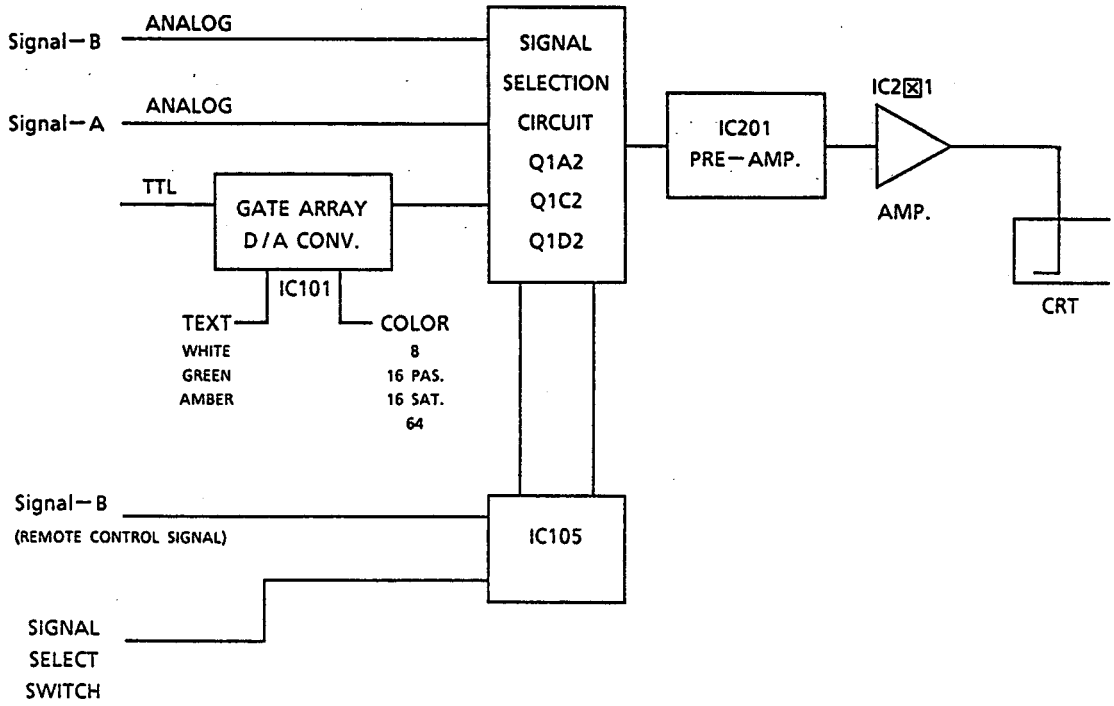
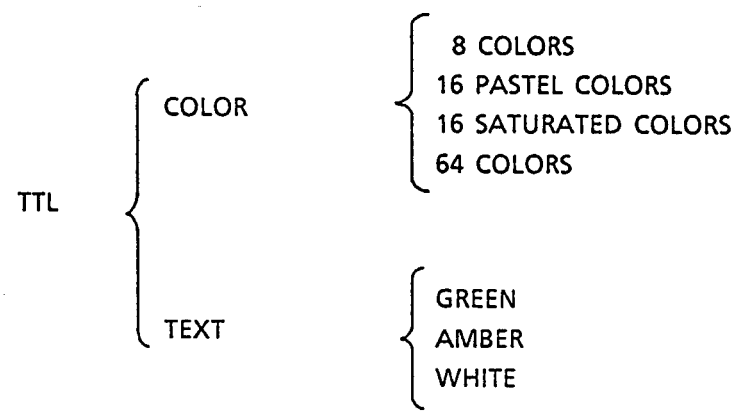


FIG. 2—6 BLOCK DIAGRAM OF VIDEO CIRCUIT

(2) PRE AMPLIFIER

(2)—1 The TTL input signal is applied to the gate array IC101, and is selectable to the following mode by MODE SELECT SWITCH on the rear panel.
The TTL signal which is converted to analog level is supplied from gate array IC101 by open collector. The converted signal is applied to the pre—amplifier IC201 via signal selection circuit.



(2)−2 The Analog signal is directly applied to the pre−amplifier IC201 via signal selection circuit. The bias and gain of video signals are controlled by front control panel via IC104 and IC105.

2.3.3 SYNC. SIGNAL

(1) AVAILABLE SYNC. SIGNAL

a. Separate and composite TTL level with positive or negative polarity at D−sub of Signal−A.

b. Separate and composite 1.5Vpp to 5.0Vpp analog level with positive or negative polarity at BNC or D −sub of Signal −B. Analog sync. signal is converted to TTL sync. signal by IC105.

c. Sync. on green with 0.3V analog level at all input connectors.

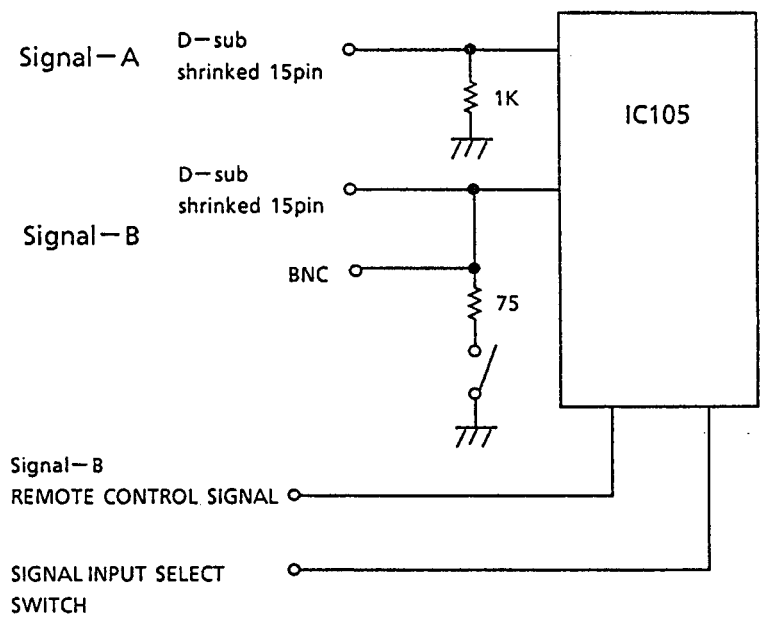


FIG. 2−7 SYNC. SIGNAL INPUT CIRCUIT

(2) CLAMP PULSE

Clamp pulse which stabilize the CRT Cut－Off level regardless of screen image is also gotten from IC105. The relation between H－sync. signal and clamp signal are as follows.

	ANALOG		TTL	
	FH＜26KHz	FH≧26KHz	FH＜26KHz	FH≧26KHz
WIDTHS	1.5μs	1.0μs	1.5μs	1.0μs
TIMING	CLAMP－B		CLAMP－A	

TABL 2－4 CLAMP PULSE WIDTH IN RELATION TO HORIZONTAL FREQUENCY

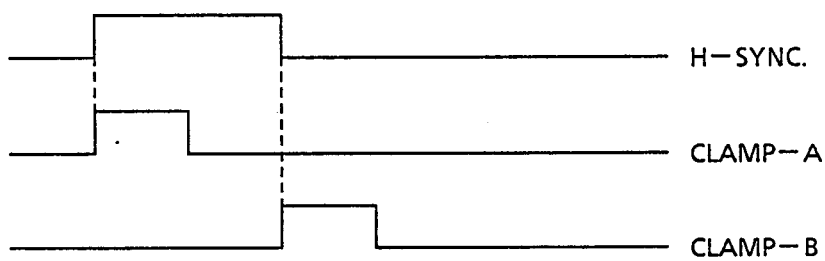


FIG. 2－8 TIME RELATION BETWEEN H－SYNC. AND CLAMP PULSE

(3) MAIN AMPLIFIER

The output of pre－amplifier is applied to the hybrid IC IC201, IC2R1, IC2G1 and IC2B1 which amplify the video levels enough to drive of CRT cathodes to 40Vpp.

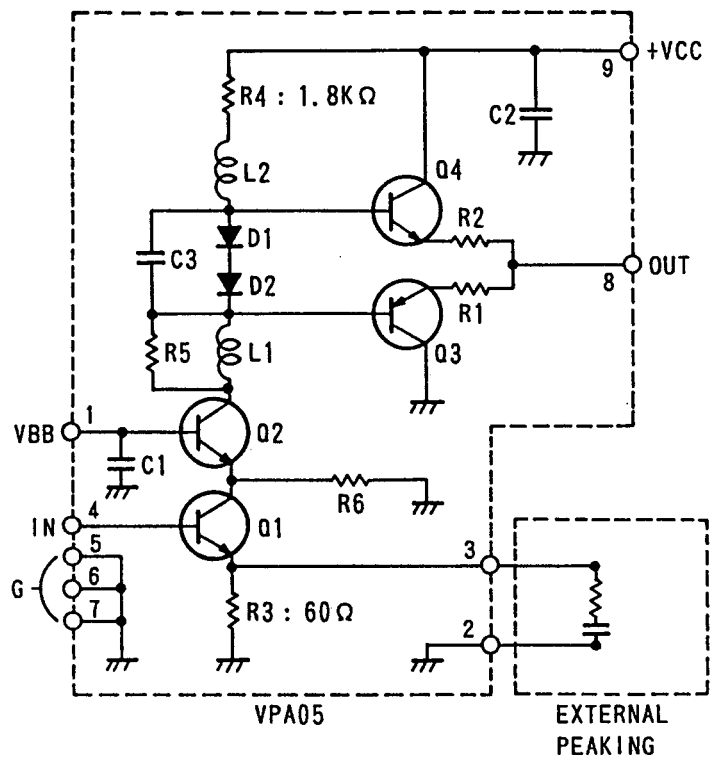


FIG. 2—9 SCHEMATIC DIAGRAM OF IC2R1, 2G1 AND 2B1

2.4 CONTROL BLOCK

(1) The control block is mainly located on the PCB－TERMINAL. It has one MPU IC104, one gate array IC105, one unvolatile memory IC106, and other control ICs.

The input signals for MPU are fed from 9 tact switches, 5 LEDs and also applied sync. signal and sync. polarity detecting signal. Based on the above signals MPU reads out data like as screen size, screen position etc. which are stored in unvolatile memory and internal ROM. These information are sent from ports of MPU. The general flow chart is shown in FIG. 2－10, and H/W block diagram is shown in FIG. 2－11. The information like as AFC constant, Cs changing and CR changing is shown in TABLE 2－5.

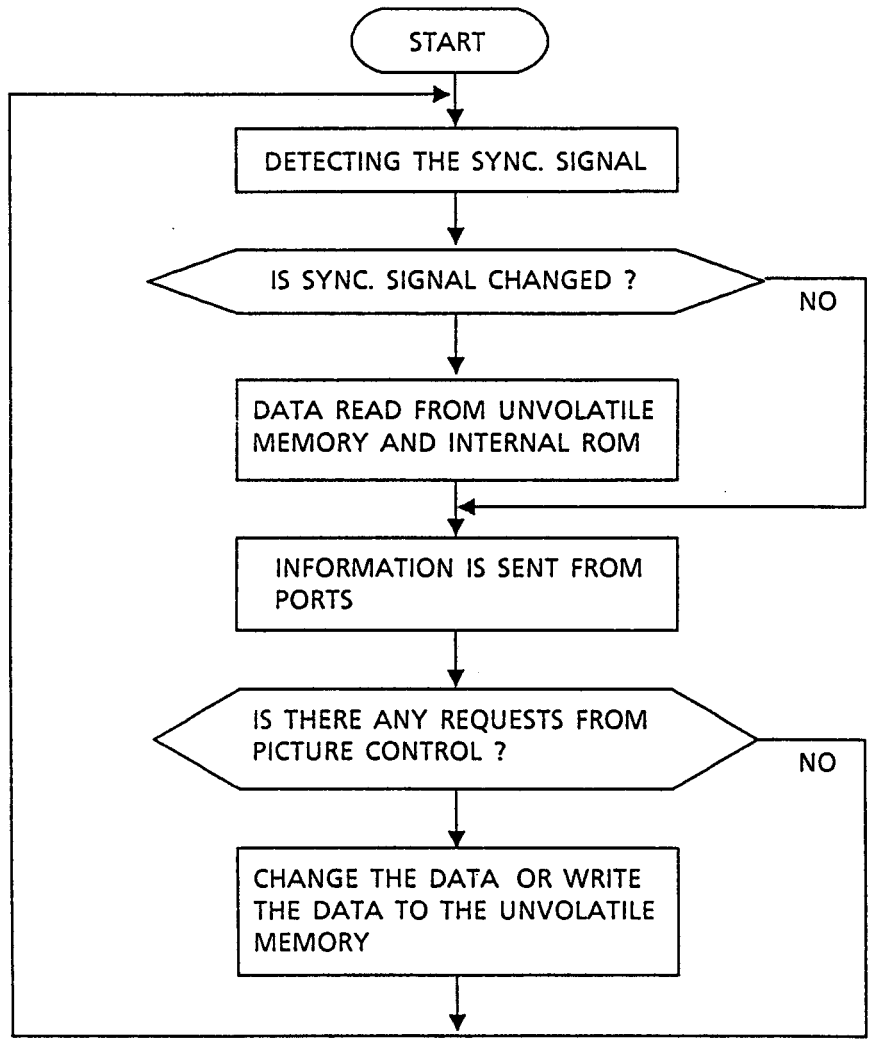

START
DETECTING THE SYNC. SIGNAL
IS SYNC. SIGNAL CHANGED ?
NO
DATA READ FROM UNVOLATILE MEMORY AND INTERNAL ROM
INFORMATION IS SENT FROM PORTS
IS THERE ANY REQUESTS FROM PICTURE CONTROL ?
NO
CHANGE THE DATA OR WRITE THE DATA TO THE UNVOLATILE MEMORY

FIG. 2－10 GENERAL FLOW CHART

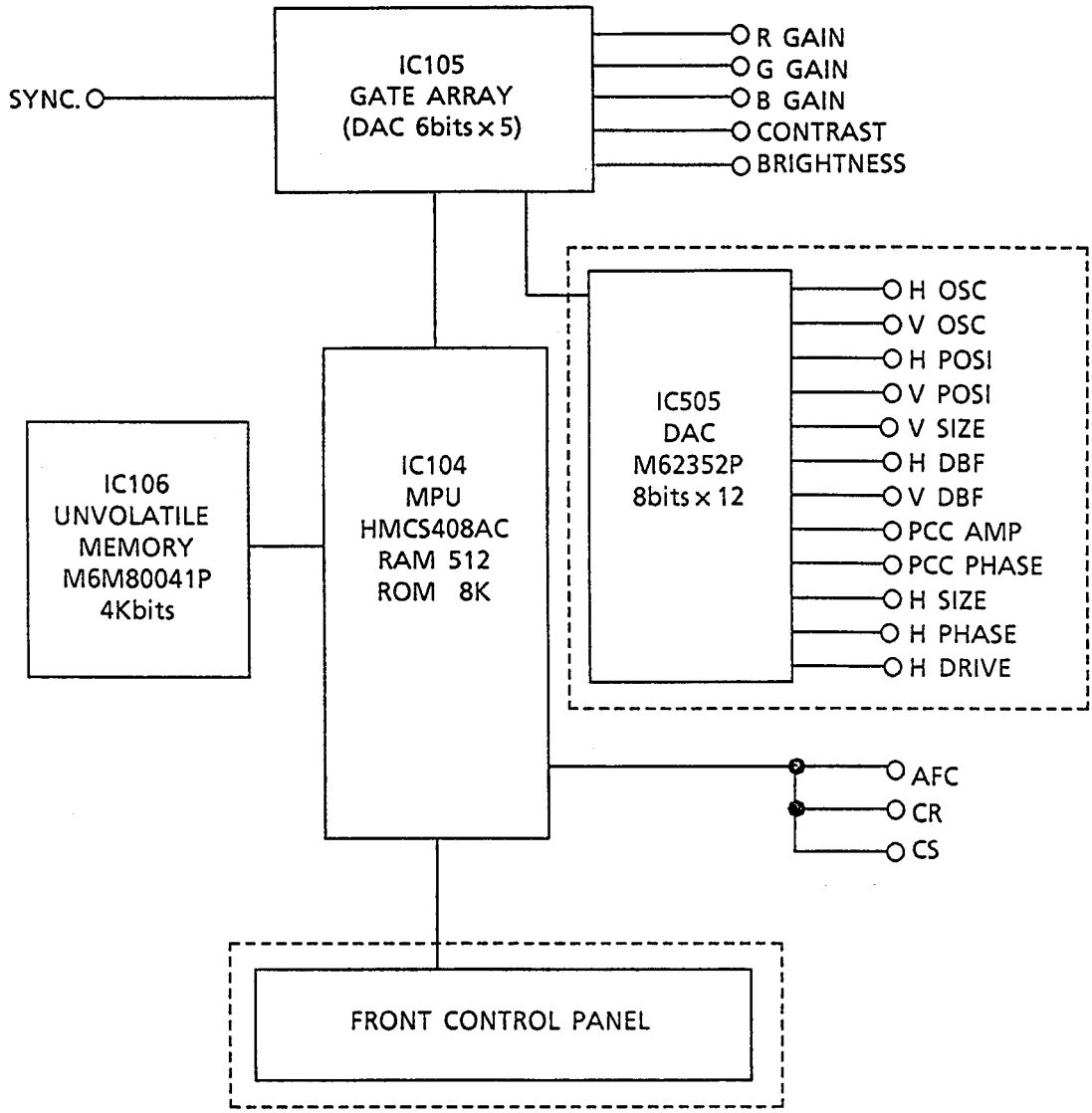


FIG. 2—11 BLOCK DIAGRAM OF CONTROL

TABLE 2—5 TRUTH TABLE OF C_S, C_R AND AFC

FH (KHz)	CS				CR			AFC	
	3	2	1	0	2	1	0	1	0
15	0	0	0	0	0	0	0	0	0
16	0	0	0	0	0	0	0	0	0
17	0	1	0	0	0	0	0	0	0
18	0	1	0	0	1	0	0	0	0
19	1	1	0	0	1	0	0	0	0
20	0	0	1	0	1	0	0	0	0
21	1	0	1	0	1	0	0	0	1
22	0	1	1	0	1	0	0	0	1
23	1	1	1	0	1	1	0	0	1
24	0	0	0	1	1	1	0	0	1
25	1	1	0	1	1	1	0	0	1
26	1	1	0	1	1	1	0	0	1
27	0	0	1	1	1	1	0	0	1
28	0	0	1	1	1	1	0	1	0
29	0	0	1	1	1	1	1	1	0
30	0	0	1	1	1	1	1	1	0
31	1	0	1	1	1	1	1	1	0
32	1	0	1	1	1	1	1	1	0
33	0	1	1	1	1	1	1	1	0
34	0	1	1	1	1	1	1	1	0
35	1	1	1	1	1	1	1	1	0
36	1	1	1	1	1	1	1	1	1
37	1	1	1	1	1	1	1	1	1
38	1	1	1	1	1	1	1	1	1

(2) IC505 is D/A converter, whose function is 8bit×12circuits, and data input is performed by serial forward. Data is sent from 54pin of IC104 to 17pin of D/A converters, and clock signal working at serial forward is applied from 55pin of IC104 to 16pin of D/A converter. Load pulse is sent from 34pin of IC104 to D/A converter, then data is maintained in latch of D/Aconverter. DC voltage from D/A converters are used to control screen width and position.

(3) IC106 is E^2PROM in which control data like screen size, position, brightness etc. can be memorized. It's function is 4Kbit. Serial data is applied from 50pin of IC104 also serial data is supplied to 51pin of IC104. These data are synchronized by clock pulse from 49pin of IC104 and transformed to 16bits data.

(4) IC105 is standard cell, that is consist of both analog and digital cells. IC105 has clock generater circuit, clump pulse generater circuit, WDT reset circuit, D/A conversion, sync. signal level convert circuit and composite sync. signal seperation circuit.

Block diagram is shown in FIG. 2—12.

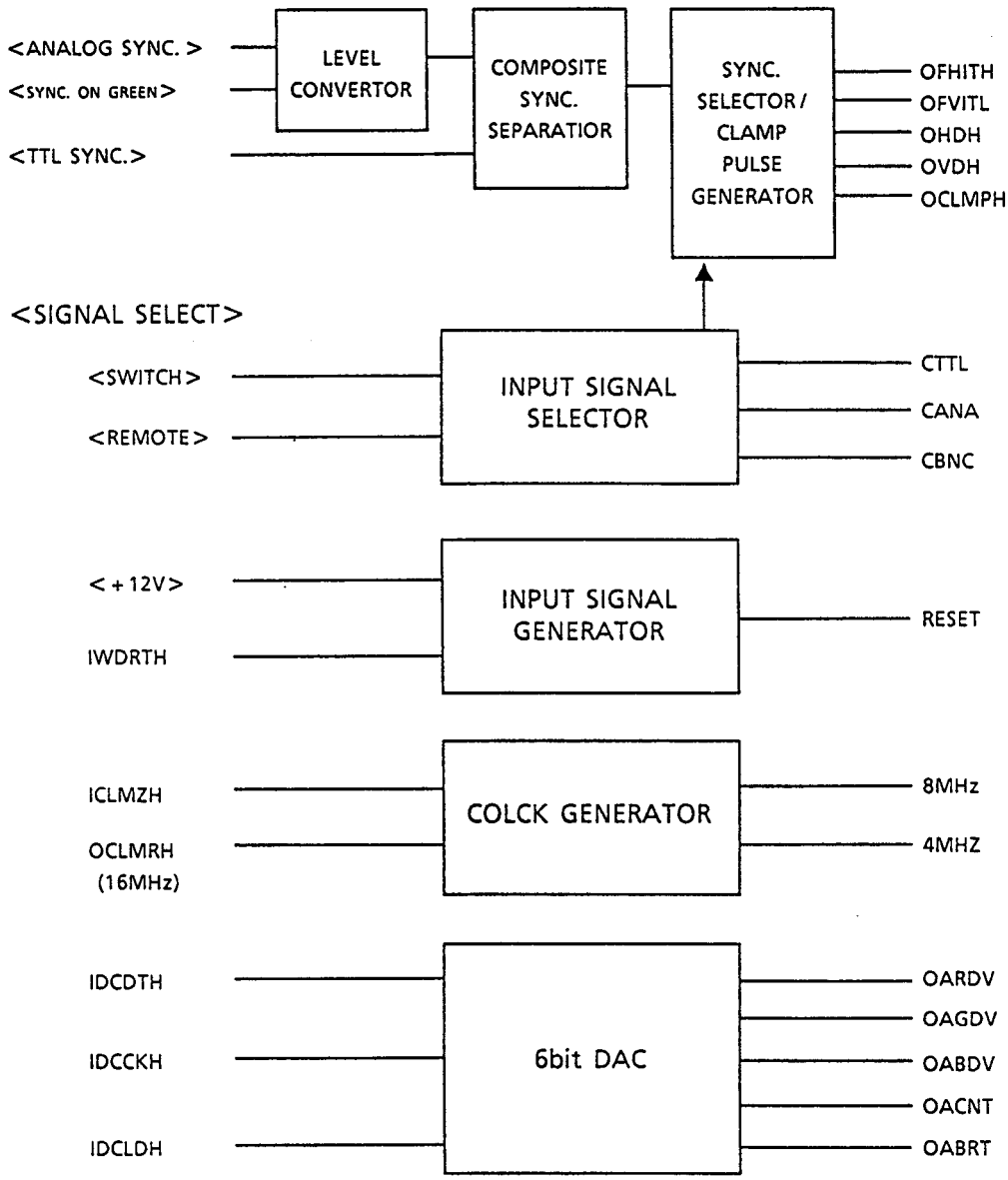


FIG. 2—12 BLOCK DIAGRAM OF STANDARD CELL

3. ADJUSTMENT PROCEDURE

This monitor is adjusted to the 8timings in PRESET MODE at factory (8timings : EGA, VGA (350Line, 400Line, 480Line), SUPER VGA (35KHz, 38KHz), MAC Ⅱ, XGA).

This monitor has 2memory areas, one is PRESET－MODE (12timings) and the other is USER －MODE (6timings). Each can be selected by changing 8th switch of MODE SELECT SWITCH on the rear panel. Upper position is USER －MODE, and lower position is PRESET－MODE. In USER－MODE 6 differrent timings can be menolized in unvolatile memory. One of conditions stated below should be satisfied to memorize 6 differrent timings.

① Horizontal synchronous frequencies are separated bigger than 2KHz to each other.

② The polarities of horizontal and / or vertical defferent to each other.

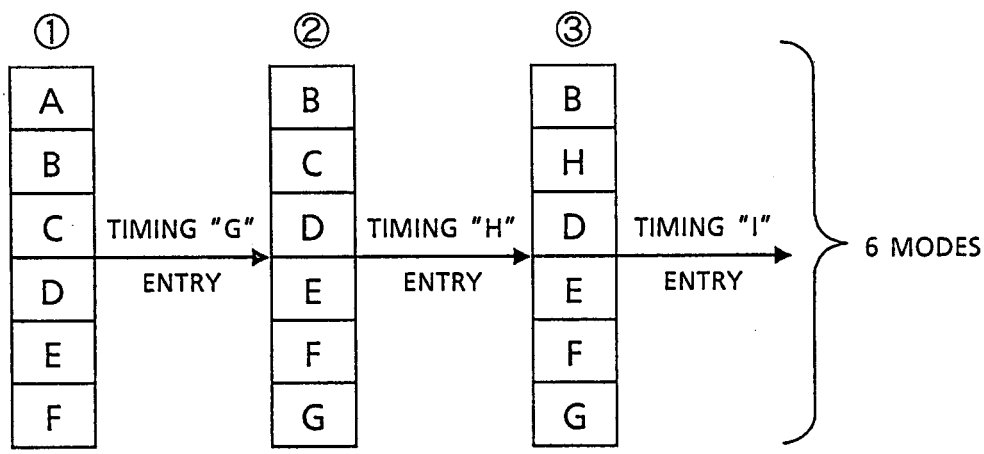
③ Vertical synchronous frequencies are separated bigger than the values stated in TABLE 3－1.

TABLE 3－1 DEVIATION OF VERTICAL FREQUENCY

45Hz~55Hz	5Hz or More
55Hz~65Hz	7Hz or More
65Hz~75Hz	10Hz or More
75Hz~90Hz	15Hz or More

<EXAMPLES>

		H−SYNC.	V−SYNC.	
31.5KHz	60Hz	+	+	DISTINUISHABLE (Polarities of sync. signal are defferent.)
31.5KHz	60Hz	+	−	
31.5KHz	60Hz	−	+	
31.5KHz	60Hz	−	−	
31.5KHz	60Hz			DISTINUISHABLE (Frequencies are separated enough.)
29.5KHz	60Hz			
29.5KHz	50Hz			



<NOTE>

① Timing "A" was memorized at first. Timing "F" was memorized at last.

② Timing "G" which can be distinguished from "A~F" can be memorized pushing timing "A" out.

③ Timing "H" which can't be distinguished from "C" can be changed with timing "C".

Re −adjustment when repairing or adjusted new timing is memorized in the unvolatile memory automatically. Almost adjustment items can be operated by 9 tact switches and 5 LEDs.

Some items like High −Voltage, CRT Cut −Off etc. can be adjusted by semifixed potentio−meters inside the monitor.

3.1 ADJUSTMENT MODE

There are three adjustment modes in this monitor.

1) NORMAL MODE
2) SERVICE MODE
3) RESERVED MODE

3.1.1 NORMAL MODE

The NORMAL MODE is used for the general end user, and is available to adjust the raster size, position, brightness and contrast by ADJUSTMENT BUTTONS on the front panel.

3.1.2 SERVICE MODE

The adjustment mode is changed from NORMAL to SERVICE by following procedure.

(1) Push both "+ / −" button of ADJUSTMENT BUTTONS then turn on the monitor.

(2) The ADJUSTMENT FUNCTION INDICATORS blinks during approx. 10sec. for the confirmation.

(3) Push both "+ / −" button of ADJUSTMENT BUTTONS, so that the ADJUSTMENT FUNCTION INDICATORS indicates V−SIZE on the front panel.

(4) If the above procedure is not finished, or push the other buttons, the NORMAL MODE is not changed to the SERVICE MODE.

The SERVICE MODE has 12 adjustment items are as follows.

ITEM NO.	ADJUSTMENT ITEM INDICATORS				ADJUSTMENT ITEM
	3	2	1	0	
1	●	●	●	○	V—SIZE
2	●	●	○	●	V—POSI
3	●	○	●	●	H—SIZE
4	○	●	●	●	H—PHASE
5	○	○	●	●	H—POSI
6	○	○	○	●	PCC—AMP
7	○	○	○	○	PCC—PHASE
8	●	○	●	○	CONTRAST
9	●	○	○	○	R—DRIVE
10	○	●	○	○	G—DRIVE
11	○	○	●	○	B—DRIVE
12	●	●	○	○	MODE SELECT SWITCH (TABLE 3—3)

○ : LED ON, ● : LED OFF

TABLE 3—2 ADJUSTMENT ITEM OF SERVICE MODE

The dip switch on the rear panel is available to set the condition of TABLE 3—3 at ITEM NO. 12 in the SERVICE MODE, which can be memorize the condition by following procedure.

(1) Push "—" button of ADJUSTMENT BUTTON.

(2) The status indicator blinks during approx. 3 sec. for the confirmation.

(3) Push both "+ / —" button of ADJUSTMENT BUTTONS. The STATUS INDICATOR become illuminate and memorized those function.

(4) If the above procedures is not finished, or push the other buttons, during the STATUS INDICATOR blinks, this operation is cancelled.

DIP SW NO.	FUNCTION	
	UPPER	LOWER
4	CLAMP REAR EDGE	CLAMP FRONT EDGE
5	SYNC. SEP. 16μs	SYNC. SEP. 12μs
6	CLAMP PULSE 0.8μs	CLAMP PULSE 1.2μs
7	SYNC. SEP. NTSC	SYNC. SEP. EOR

TABLE 3—3 FUNCTION OF MODE SELECT SWITCH

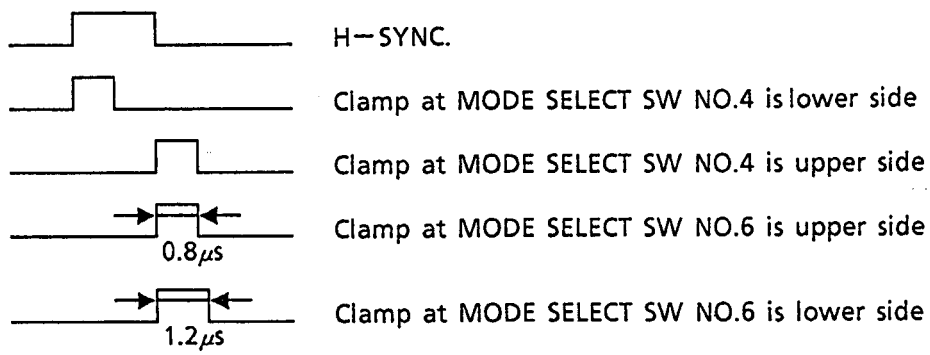

H—SYNC.
Clamp at MODE SELECT SW NO.4 is lower side
Clamp at MODE SELECT SW NO.4 is upper side
Clamp at MODE SELECT SW NO.6 is upper side
0.8μs
Clamp at MODE SELECT SW NO.6 is lower side
1.2μs

FIG. 3—1 CLAMP PULSE

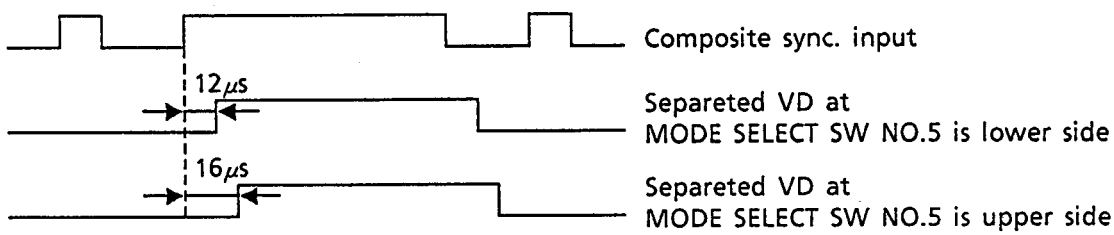


FIG. 3—2 COMPOSITE SYNC. SEPARETE TIMING

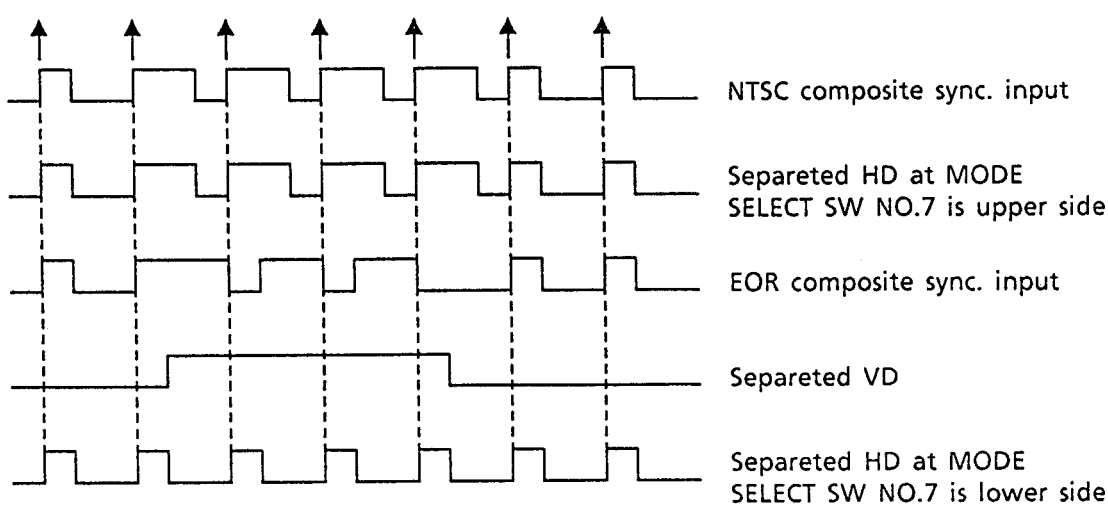

NTSC composite sync. input
Separeted HD at MODE
SELECT SW NO.7 is upper side
EOR composite sync. input
Separeted VD
Separeted HD at MODE
SELECT SW NO.7 is lower side

FIG. 3—3 COMPOSITE SYNC. SEPARETE TYPE

3.1.3 RESERVED MODE

The adjustment mode is changed from NORMAL to RESERVED by following procedure.

(1) Push "+" button of CONTRAST CONTROL and push "−" button of BRIGHTNESS CONTROL at same time then turn on the monitor.

(2) The STATUS INDICATOR blinks during approx. 10sec. for the confirmation so the ADJUSTMENT ITEM INDICATORS (○○○○).

(3) Select the indication (○●○●) of ADJUSTMENT ITEM INDICATORS by the ADJUSTMENT FUNCTION SELECT BUTTONS.

(4) Push both "+ / −" button of ADJUSTMENT BUTTONS.

(5) If the above procedure is not finished, or push the other buttons, during the INDICATOR blinks, the NORMAL MODE is not changed to the RESERVED MODE.

The RESERVED MODE has 16adjustment items shown TABLE 3 −4. And adjustment data can be memorized not only user memory but also factory memory.

All user timing (USER MODE) can be elased is following operation.

(1) Select item NO. 12 by ADJUSTMENT FUNCTION SELECT BUTTONS.

(2) Push "+" button of ADJUSTMENT BUTTON.

(3) The STATUS INDICATOR blinks during approx. 3sec. for the confirmation.

(4) Push both "+ / −" button of ADJUSTMENT BUTTONS.

(5) If the above procedure is not finished, or push the other bottuns, during the STATUS INDICATOR blinks, this operation is cancelled.

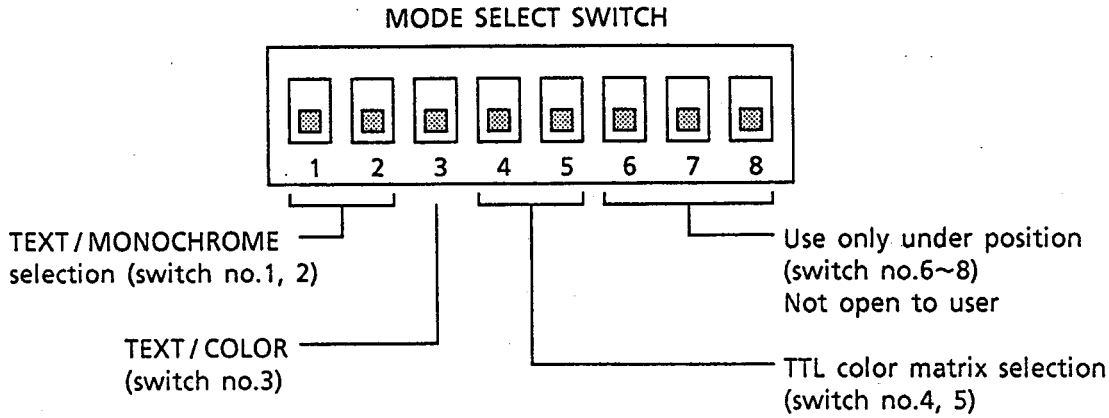
The RESERVED MODE is preset timing use only.

ITEM NO.	ADJUSTMENT ITEM INDICATORS				ADJUSTMENT ITEM
	3	2	1	0	
1	●	●	●	○	V—SIZE
2	●	●	○	●	V—POSI
3	●	○	●	●	H—SIZE
4	○	●	●	●	H—PHASE
5	○	○	●	●	H—POSI
6	○	○	○	●	PCC—AMP
7	○	○	○	○	PCC—PHASE
8	●	○	●	○	CONTRAST
9	●	○	○	○	R—DRIVE
10	○	●	○	○	G—DRIVE
11	○	○	●	○	B—DRIVE
12	●	●	○	○	USER TIMING ELASE
13	●	○	○	●	V—OSC 45
14	○	●	●	○	V—OSC 95
15	●	●	●	●	H—DBF
16	○	●	○	●	V—DBF

○ : LED ON, ● : LED OFF

TABLE 3—4 ADJUSTMENT ITEM OF RESERVED MODE

3.2 MODE SELECT SWITCH



3.2.1 TEXT / MONOCHROME SELECTION (SWITCH NO.1, 2)

Tihs can be on TTL mode and select three color on the TEXT position.

Examples of selection is following switch position.

COLOR	GREEN	AMBER	WHITE
SWITCH POSITION	1 2	1 2	1 2

3.2.2 TEXT COLOR SWITCH (SWITCH NO.3)

This can be used on TTL mode only, and has 3 text colors of green, amber and white.

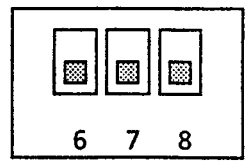
3.2.3 TTL COLOR MATRIX SELECTION (SWITCH NO.4, 5)

Under PRESET MODE condition, this can be select following 4 colors when you select color switch on TTL mode prior to connecting with your parsonal computer, and memorized to the unvolatiale memory. EGA signal is fixed 64colors automatically.

COLOR	8 colors	16 COLORS SATURATION	16 COLORS PASTEL	64 COLOS
SWITCH POSITION	4 5	4 5	4 5	4 5

Under USER MODE condition, TTL color is selected by unvolatiale memory instead of these switch.

3.2.4 USE ONLY UNDER POSITION (SWITCH NO.6~8)



These function are not open to user.

① COLOR TEMPERATURE SELECT SWITCH (SWITCH NO.6)

Lower position : Adjusted 9300°K by factory

Upper position : Another color temperature such as 6550°K is adjustable

② RECALL MODE SELECT SWITCH (SWITCH NO.7)

Lower position : Restore the factory standard data by pressing recall switch

Upper position : Alternate PRESET MODE and USER MODE by pressing recall switch.

③ SACN MODE SELECT SWITCH (SWITCH NO.8)

Lower position : PRESET MODE

applied signal is compared with preset timing first which is stored unvolatile memory by MPU. If MPU can not detect same timing in the stored preset timing, then compare with user timing.

Upper position : USER MODE

applied signal is compared with user timing first which is stored unvolatile memory by MPU. If MPU can not detect same timing in the stored user timing, then compare with preset timing.

3.3 INTERNAL ADJUSTMENT

3.3.1 HORIZONTAL FREE RUNNING FREQUENCY ADJUSTMENT

(1) Connect the frequency counter between red cable of DY and chassis ground.

(2) Set SW201 on the PCB−TERMINAL to FRN position.

(3) Receive 39KHz sync. signal, and adjust the horizontal free running frequency for a 39.0 ± 0.2KHz by VR505 (H−HOLD 2) on the PCB−DEFL.

(4) Receive 15.7KHz sync. signal, and adjust the horizontal free running frequency for a 15.7 ± 0.2KHz by VR501 (H−HOLD 1) on the PCB−DEFL.

(5) After above adjustment, check 39.0KHz horizontal frequency, then if neccessary, re-adjust the adjustment procedure of item (3) and (4).

(6) Set SW201 to center position.

3.3.2 VERTICAL FREE RUNNING FREQUENCY ADJUSTMENT

(1) Connect the frequency counter between the terminal of vertical coil on DY and chassis ground.

(2) To select the adjustment item of V－OSC 45 and V－OSC 95, the RESERVED MODE should be selected according to the procedure stated in the paragraph of RESERVED MODE.

(3) Set SW201 on the PCB－TERMINAL to FRN position.

(4) Select the adjustment item of V－OSC 45 by ADJUSTMENT FUNCTION SELECT BUTTON on the front panel.

(5) Adjust the vertical free running frequency for a 38.0±2Hz by ADJUSTMENT BUTTON.

(6) Select the adjustment item of V－OSC 95 by ADJUSTMENT FUNCTION SELECT BUTTON on the front panel.

(7) Adjust the vertical free running frequency for a 85.0±2Hz by ADJUSTMENT BUTTONS.

(8) Set SW201 to center position.

3.3.3 HIGH VOLTAGE PROTECTOR ADJUSTMENT (VGA400Line)

(1) Connect the high voltmeter (full scale bigger than 35KV) between CRT anode and chassis ground.

(2) Receive VGA400Line signal with full white pattern.

(3) Turn the SCREEN control on FBT to fully clockwise position.

(4) Adjust the high voltage for a 30.0±0.3KV by VR503 (HV－ADJ).

(5) Turn slowly VR504 (HV－PRO) to obtain the shut down point of high voltage protector.

(6) Turn off the monitor, then turn VR503 (HV－ADJ) to fully counter clockwise position.

(7) Turn on the monitor, then turn VR503 (HV－ADJ) to confirm the shut doun point at 30.0±0.3KV.

(8) If neccessary, an adhesive may be used for fixing the VR504 (HV－PRO) after adjustment.

3.3.4 HIGH VOLTAGE ADJUSTMENT (VGA400Line)

(1) Connect the high voltmeter between CRT anode and chassis ground.

(2) Receive VGA400Line signal with full white pattern.

(3) Adjust the high voltage for a 27.0±0.3KV by VR503 (HV－ADJ).

(4) If neccessary, an adhesive may be used for fixing the VR503 (HV－ADJ) after adjustment.

CAUTION

HV−ADJ (VR503) and HV−PRO (VR504) controls are sealed and no field serviceable parts to avoid exposure of X−Ray.

Please contact to qualified personnal of Mitsubishi, if necessary to re−adjust.

3.3.5 SCREEN VOLTAGE ADJUSTMENT (VGA400Line)

(1) Connect the high voltmeter between TP −SC on the PCB −CRT and chassis ground.

(2) Adjust the screen voltage for a 570 ± 10V by SCREEN control on FBT.

CAUTION

SCREEN control of FBT is also sealed by adhesive.

Please contact to qualified personnel of Mitsubishi, if necessary to re−adjust.

3.3.6 HORIZONTAL DRIVE ADJUSTMENT (VGA400Line)

(1) Connect the voltmeter between C965 (+ side) and chassis ground.

(2) Adjust VR502 (H −DRIVE) to obtain the minimum voltage reading on the voltmeter.

3.3.7 CRT CUT−OFF ADJUSTMENT (VGA400Line)

(1) Receive VGA400Line signal with no raster.

(2) Set the CONTRAST control to maximum, and the BRIGHTNESS control to center value (push both "+ / −" button at the same time for the center value).

(3) Turn VR6R1 (R−CUT−OFF), VR6G1 (G−CUT−OFF), VR6B1 (B−CUT−OFF) to their fully clockwise positions.

(4) Adjust the VR601 (G1−ADJ) on the PCB−CRT slowly so that either, green or bule back ground begins to appear.

(5) Adjust each CUT −OFF control (VR6R1, VR6G1 and VR6G1) so a white back ground shines slightly.

(6) Adjust the VR601 (G1−ADJ) on the PCB−CRT for a 1.0cd/m^2 (nits) reading on the luminace meter.

3.3.8 WHITE BALANCE ADJUSTMENT (VGA350Line)

(1) To select the adjustment item of R, G, B — DRIVE, the SERVICE MODE should be selected according to the procedure stated in the paragraph of SERVICE MODE.

(2) Set the CONTRAST control on the front panel to its maximum value.

(3) Select the CONTRAST (Adjustment item indicators : ●○●○) by ADJUSTMENT FUNCTION SELECT BUTTON, and adjust the CONTRAST by ADJUSTMENT BUTTONS so the contrast is maximum.

(4) Receive a 80×80mm square window pattern signal on the center of screen.

(5) Select the DRIVE controls by ADJUSTMENT FUNCTION SELECT BUTTON, and adjust the drive by ADJUSTMENT BUTTONS for a standard white as follows. If neccessary, a color analyzer maybe used.

	ADJUSTMENT ITEM INDICATORS	LUMINANCE cd / m² (nits)	LUMINANCE cd / m² (nits)
RED	●○○○	15.7	
GREEN	○●○○	80 ± 5	45 ± 5
BLUE	○○●○	6.1	
COLOR CORDINATION	X	0.283 ± 0.02	0.283 ± 0.02
	Y	0.297 ± 0.02	0.297 ± 0.02
CRT TYPE		SPB22	SPBL9

TABLE 3—5

3.4 RASTER ADJUSTMENT

3.4.1 GENERAL

(1) When adjust the raster condition, the SERVICE MODE should be selected according to the procedure stated in.

(2) Adjustment item of raster condition can be selected by the ADJUSTMENT FUNCTION SELECT BUTTONS on the front panel, and indication of LED is as follows.

ADJUSTMENT ITEM	ADJUSTMENT FUNCTION INDICATORS
V−SIZE	●●●○
V−POSI	●●○●
H−SIZE	●○●●
H−PHASE	○●●●
H−POSI	○○●●
PCC−AMP	○○○●
PCC−PHASE	○○○○

○ : LED ON ● : LED OFF

TABLE 3−6

3.4.2 HORIZONTAL POSITION ADJUSTMENT

(1) Receive only sync. signal (no raster).

(2) Set S201 on the PCB−TERMINAL to raster position.

(3) Select the H−POSI by ADJUSTMENT FUNCTION SELECT BUTTON on the front panel.

(4) Adjust the horizontal raster position by ADJUSTMENT BUTTONS so the back ground is positioned in the center of the CRT.

3.4.3 PCC ADJUSTMENT

(1) Receive a full white raster pattern signal.

(2) Select the PCC −AMP and PCC −PHASE by ADJUSTMENT FUNCTION SELECT BUTTON on the front panel.

(3) Adjust the PCC −AMP and PCC −PHASE by ADJUSTMENT BUTTONS to obtain the straight raster.

3.4.4 HORIZONTAL WIDTH AND PHASE ADJUSTMENT

(1) Receive a full white raster pattern signal.

(2) Select the H−WIDTH by ADJUSTMENT SELECT FUNCTION BUTTON, and adjust the horizontal width by ADJUSTMENT BUTTONS so the width is 350 ± 10mm.

(3) Select the H−PHASE by ADJUSTMENT FUNCTION SELECT BUTTON, and adjust the horizontal phase by ADJUSTMENT BUTTONS so the raster is positioned in the center of the CRT screen.

3.4.5 VERTICAL HEIGHT AND POSITION ADJUSTMENT

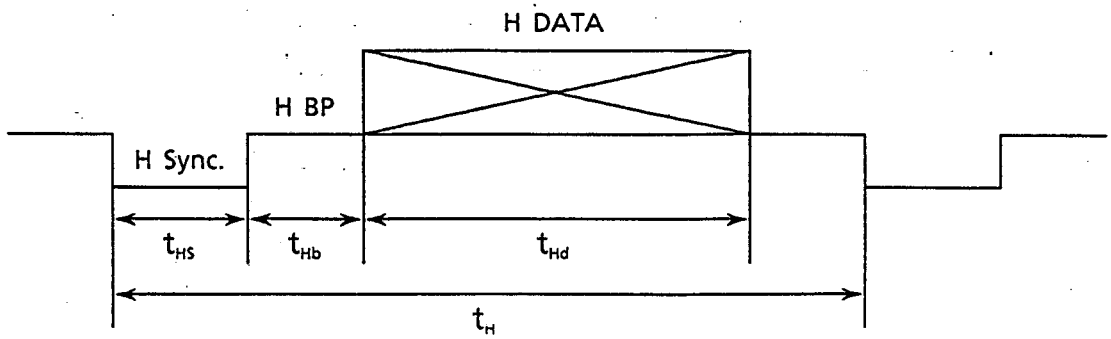
(1) Receive a full white raster pattern signal.

(2) Select the V−SIZE by ADJUSTMENT FUNCTION SELECT BUTTON, and adjust the vertical height by ADJUSTMENT BUTTONS so the height is 265 ± 10mm.

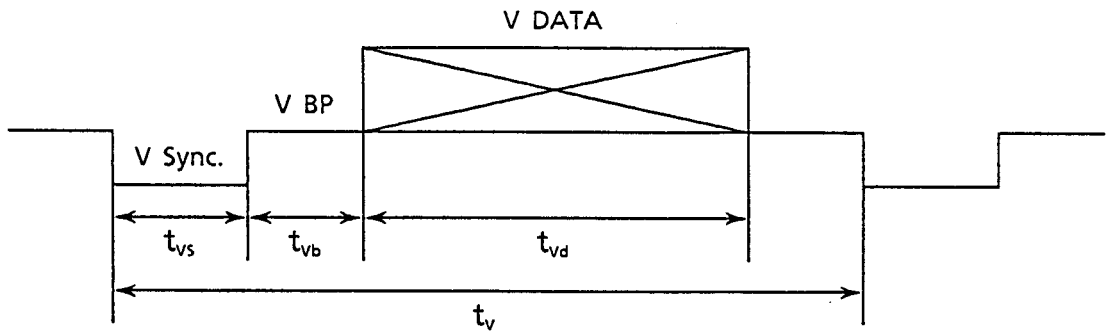
(3) Select the V −POSI by ADJUSTMENT FUNCTION SELECT BUTTON, and adjust the vertical position by ADJUSTMENT BUTTONS so the raster is positioned in the center of the CRT screen.

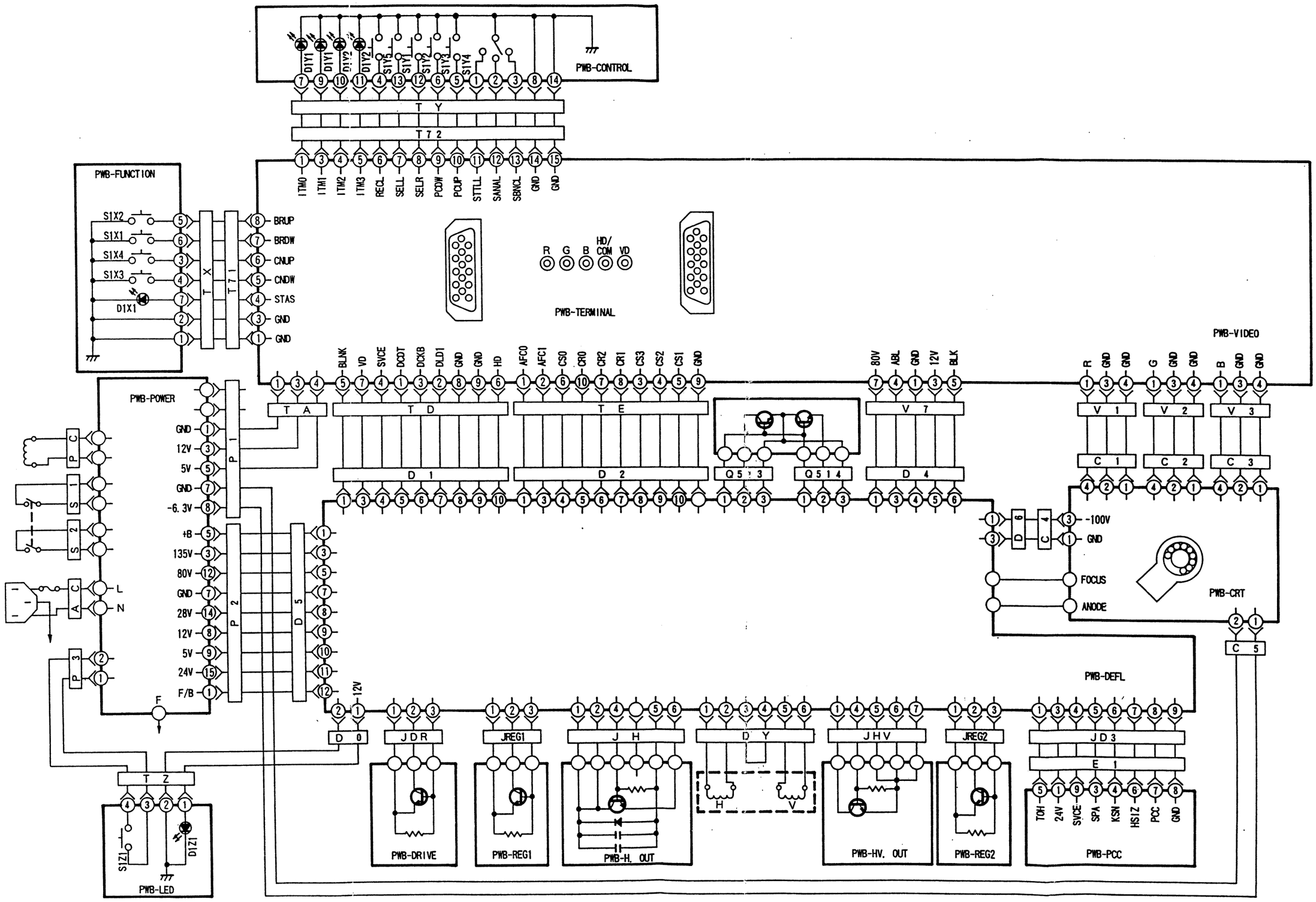
TIMING CHART

(1) HORIZONTAL (1H)



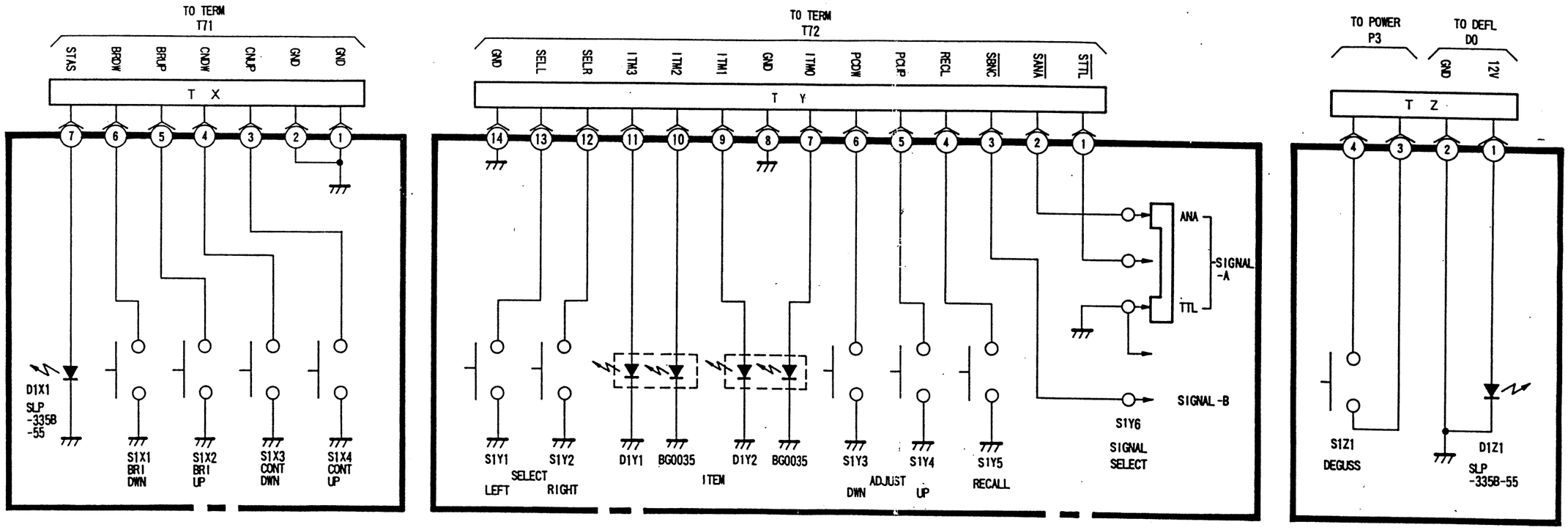
(2) VERTICAL (1V)





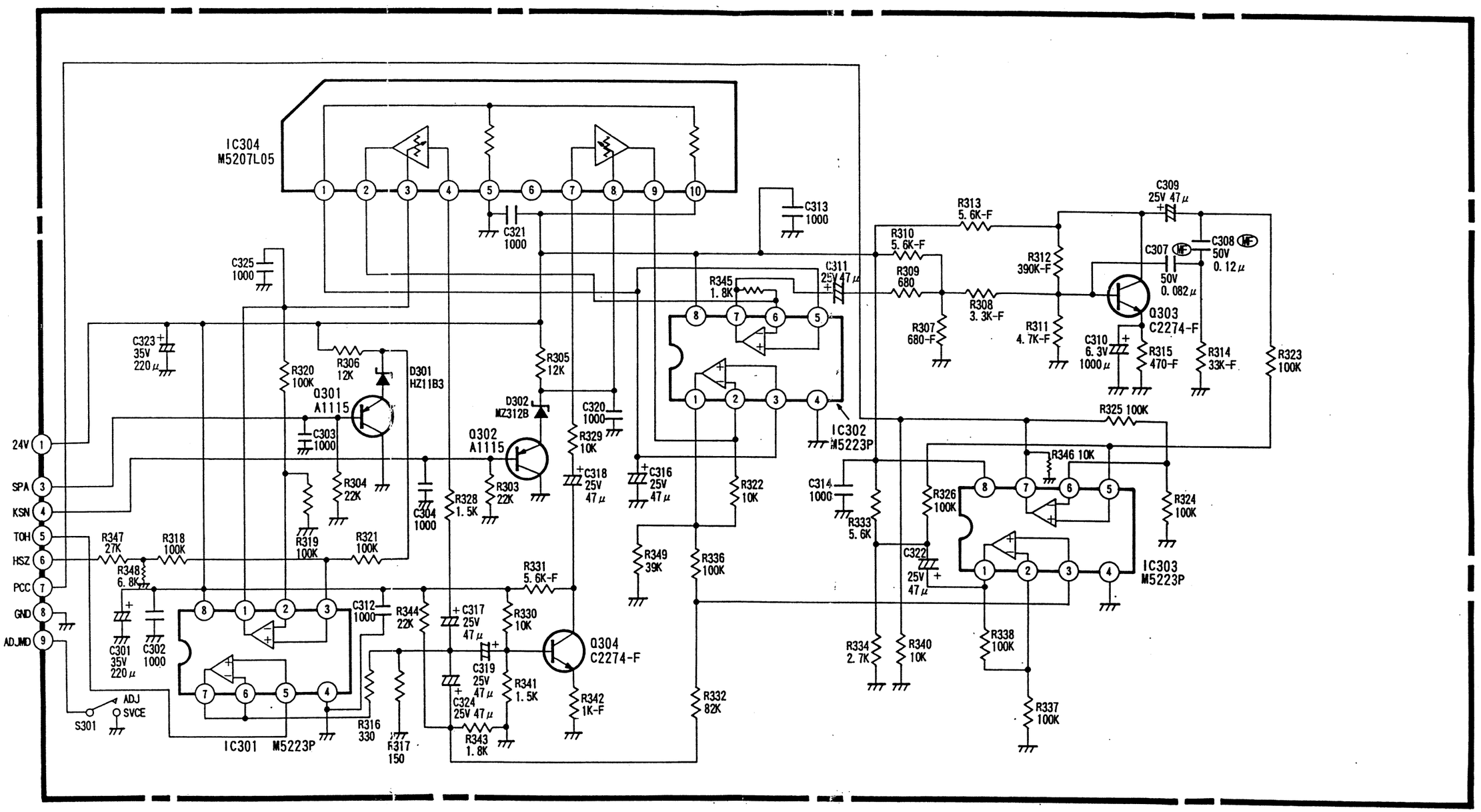
MODEL:HC3925

BLOCK DIAGRAM



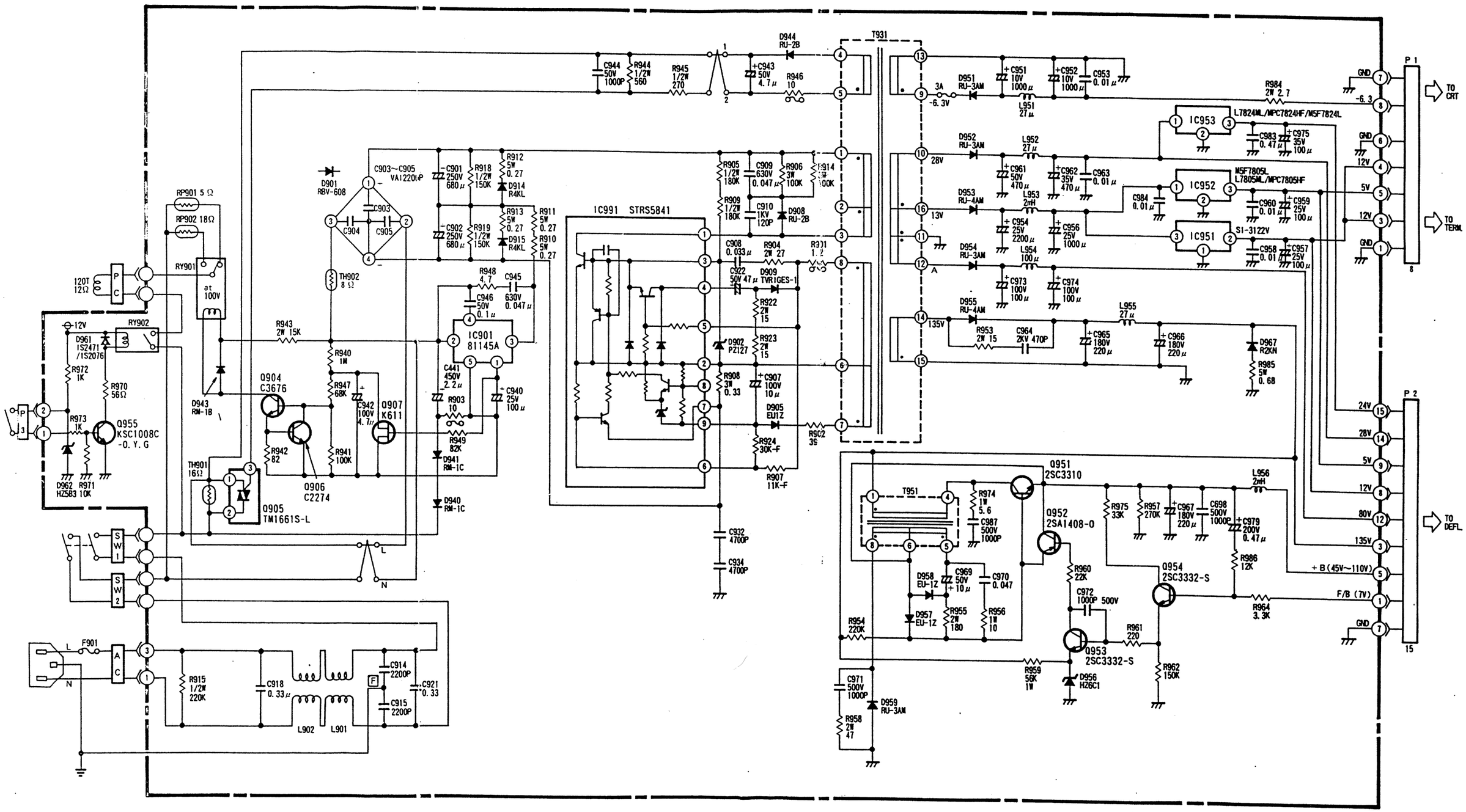
MODEL:HC3925

FRONT CONTROL CIRCUIT

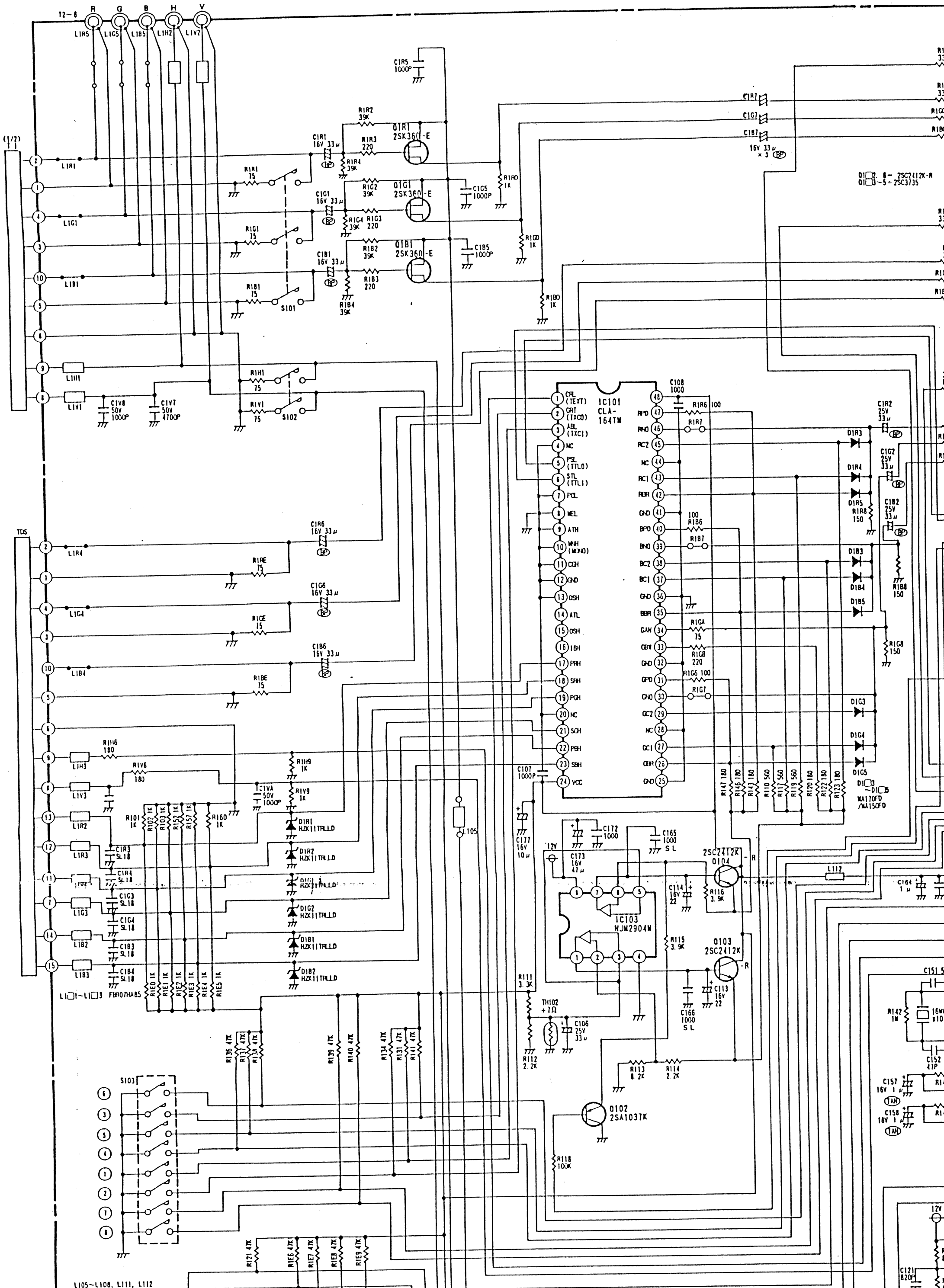


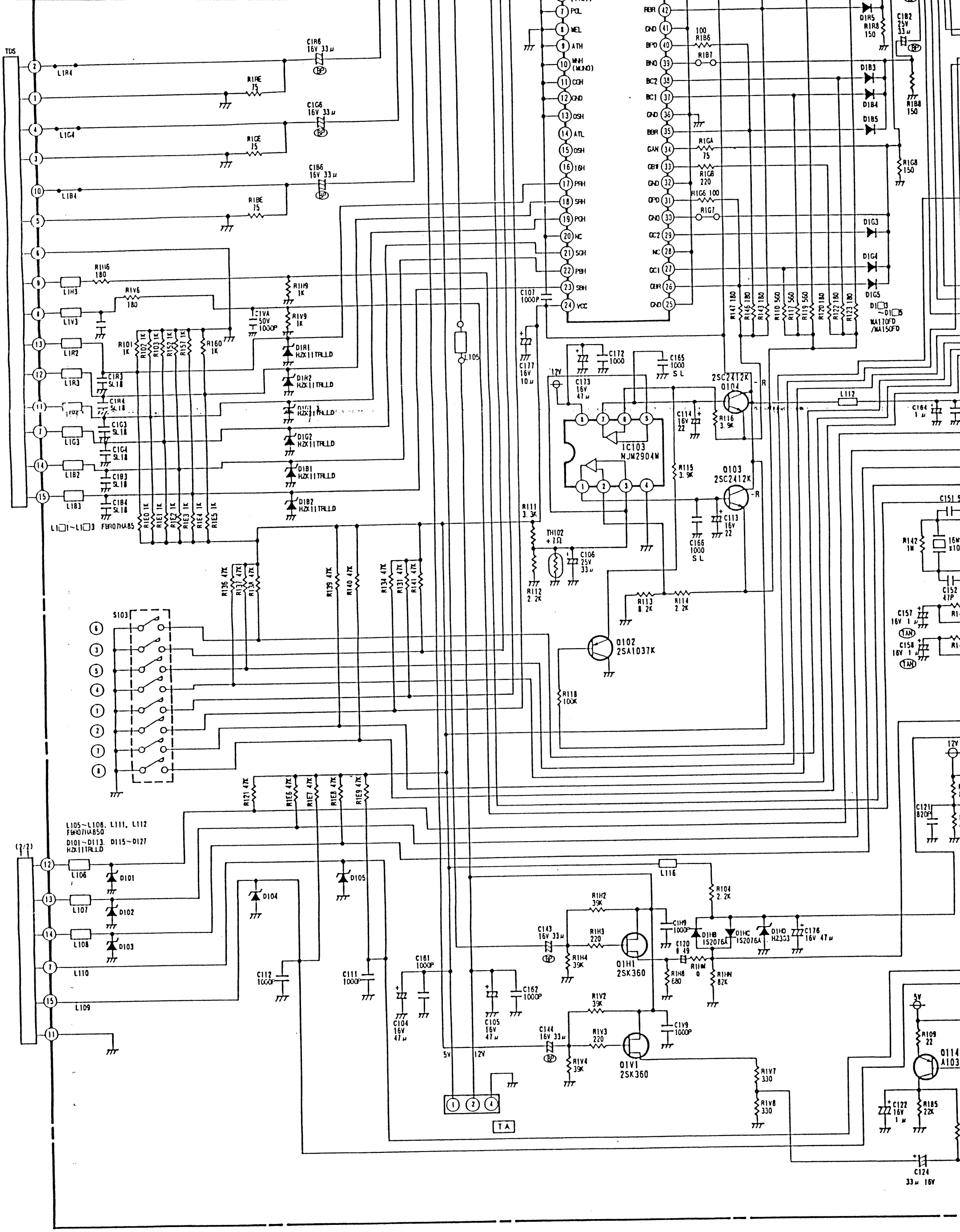
MODEL:HC3925

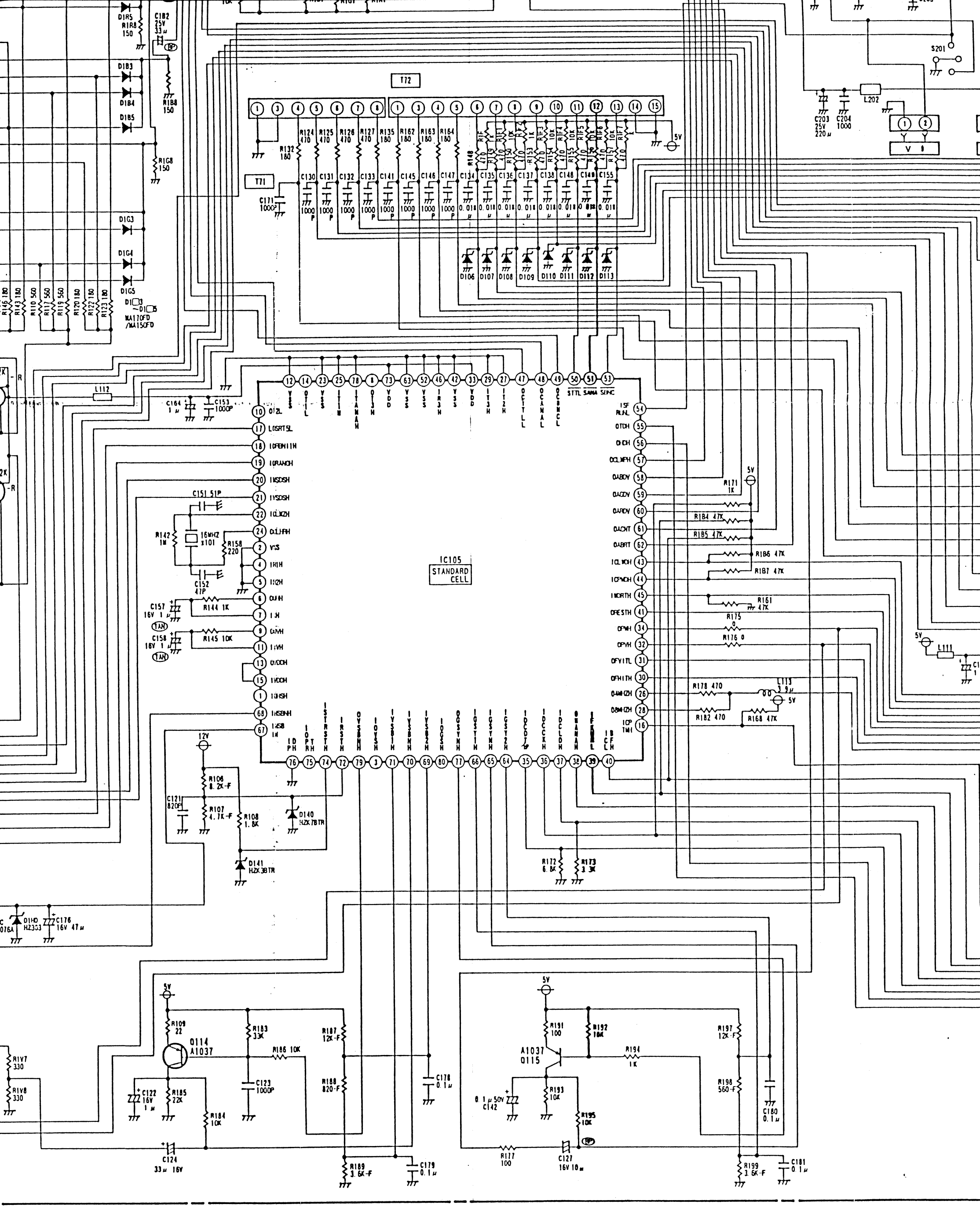
PCC CIRCUIT

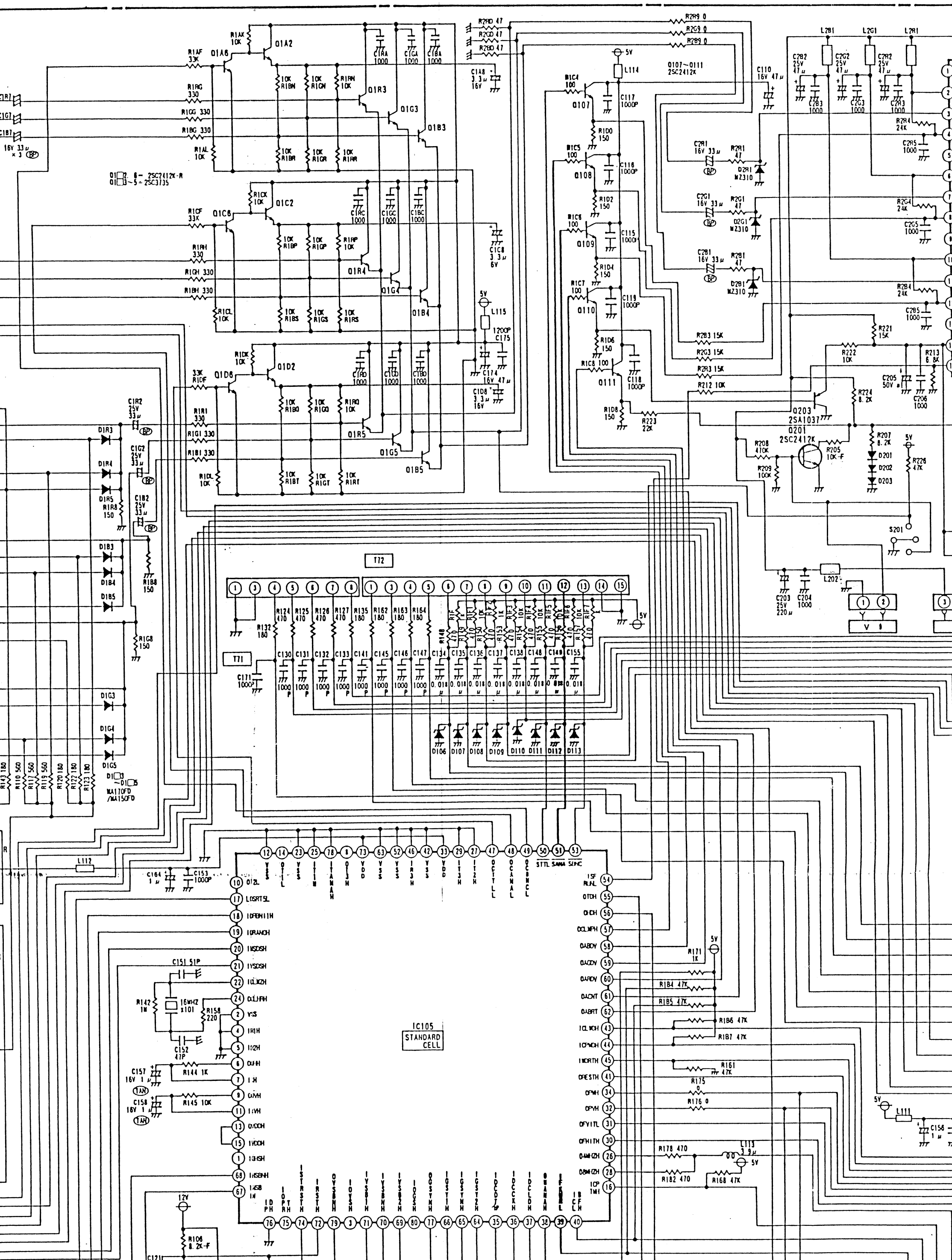


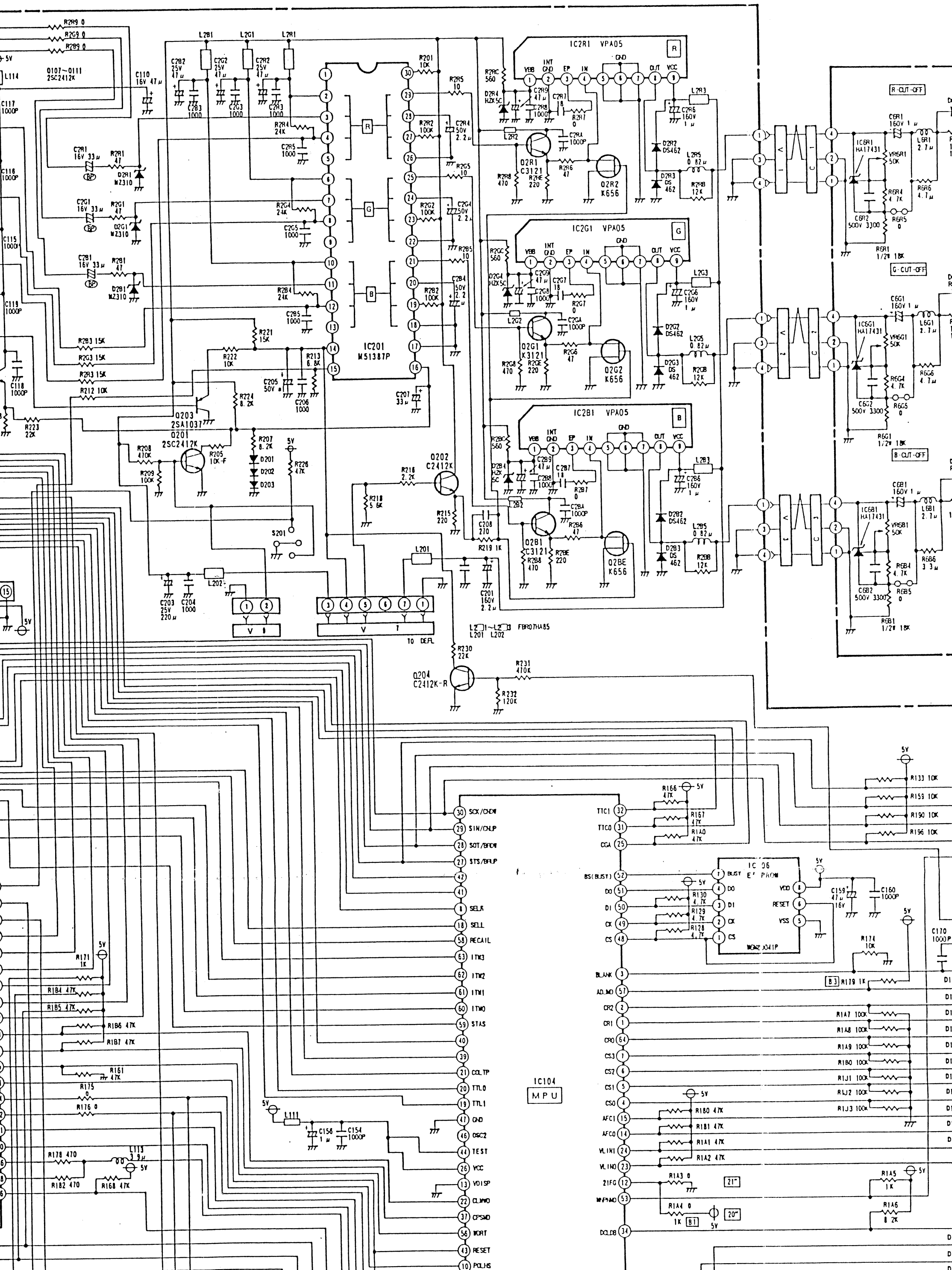
VIDE-V24441 / Druck 4

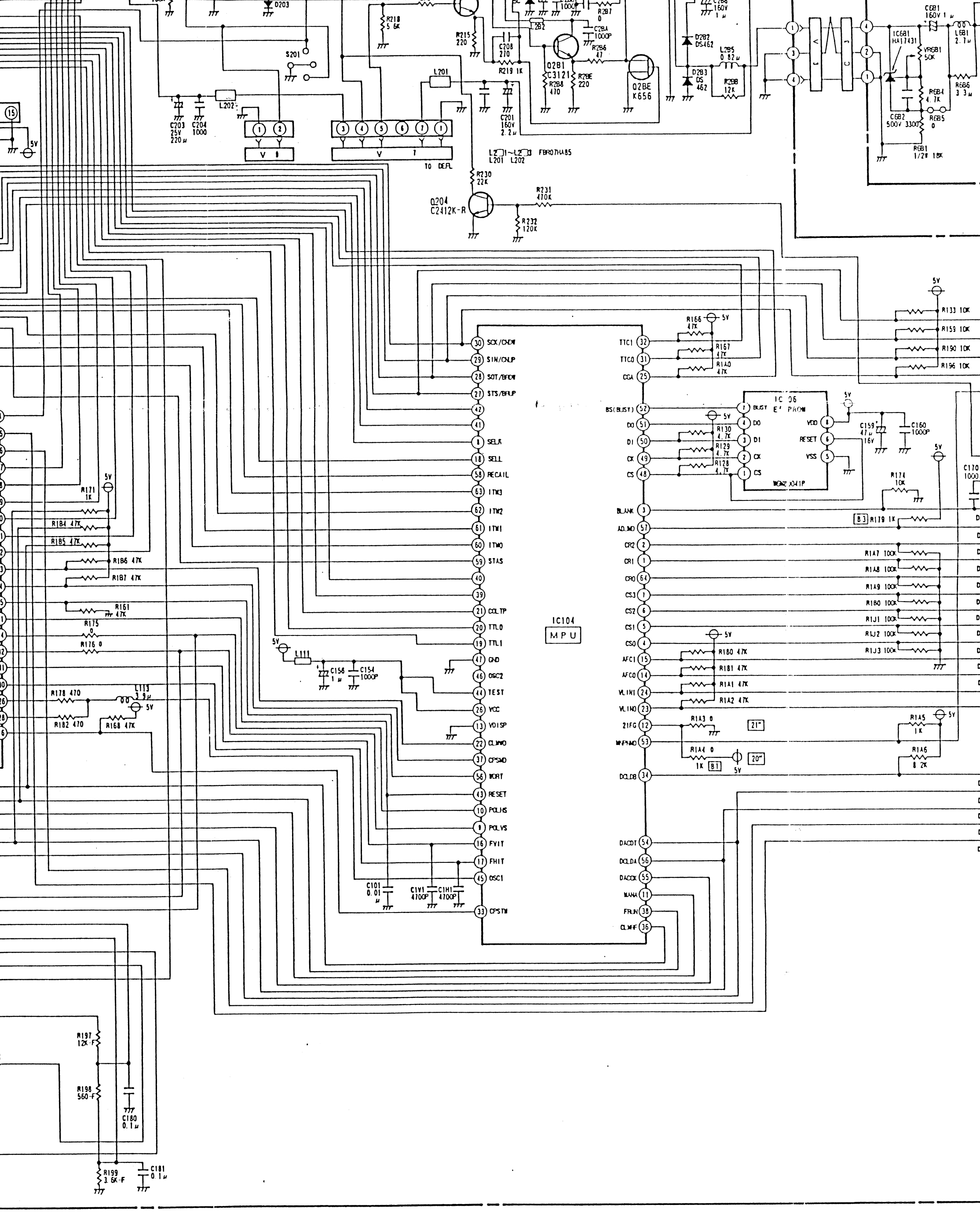

T2~6
R
G
B
H
V
L1R5
L1G5
L1B5
L1H2
L1V2
(1/2)
L1R1
L1G1
L1B1
L1H1
L1V1
C1V8 50V 1000P
C1V7 50V 4700P
R1R1 75
R1G1 75
R1B1 75
R1V1 75
S101
S102
C1R5 1000P
R1R2 39K
R1R3 220
R1R4 39K
C1R1 16V 33μ
Q1R1 2SK360-E
R1G2 39K
R1G4 39K
R1G3 220
C1G1 16V 33μ
Q1G1 2SK360-E
R1B2 39K
R1B3 220
R1B4 39K
C1B1 16V 33μ
Q1B1 2SK360-E
C1G5 1000P
C1B5 1000P
R1R0 1K
R1G0 1K
R1B0 1K
C1R7
C1G7
C1B7
16V 33μ ×3
Q1□2, 4~2SC2412K-R
Q1□3~5=2SC3735
TO5
L1R4
L1G4
L1B4
L1H3
L1V3
L1R2
L1R3
L1G3
L1B2
L1B3
L1□1~L1□3 FERRITE BEAD
R1RE 75
R1GE 75
R1BE 75
C1R6 16V 33μ
C1G6 16V 33μ
C1B6 16V 33μ
R1116 180
R1V6 180
R1119 1K
R1V9 1K
C1VA 50V 1000P
R1101 1K
R1102 1K
R1103 1K
R152 1K
R157 1K
R160 1K
R1E0 1K
R1E1 1K
R1E2 1K
R1E3 1K
R1E4 1K
R1E5 1K
C1R3 SL1B
C1R4 SL1B
C1G3 SL1B
C1G4 SL1B
C1B3 SL1B
C1B4 SL1B
D1R1 HZK11TRLLD
D1R2 HZK11TRLLD
D1G1 HZK11TRLLD
D1G2 HZK11TRLLD
D1B1 HZK11TRLLD
D1B2 HZK11TRLLD
IC101 CLA-164TM
CRL (TEXT)
CRT (TXC0)
ABL (TXC1)
NC
PSL (TTL0)
STL (TTL1)
PCL
MEL
ATH
MNH (MONO)
CCH
GND
OSH
ATL
OSH
16H
PRH
SRH
PGH
NC
SGH
PBH
SBH
VCC
C108 1000
R1R6 100
R1R7
R1G6 100
R1G7
R1B6 100
R1B7
R1GA 75
R1GB 220
R1G8 150
R1B8 150
C1R2 25V 33μ
C1G2 25V 33μ
C1B2 25V 33μ
D1R3
D1R4
D1R5
R1R8 150
D1B3
D1B4
D1B5
D1G3
D1G4
D1G5
D1□3~D1□5 MA170FD /MA150FD
R147 180
R146 180
R143 180
R110 560
R117 560
R119 560
R120 180
R122 180
R123 180
C107 1000P
C177 16V 10μ
L105
12V
C172 1000
C173 16V 47μ
C165 1000 SL
2SC2412K Q104 -R
L112
C164 1μ
C114 16V 22
R116 3.9K
IC103 NJM2904M
R115 3.9K
Q103 2SC2412K -R
C113 16V 22
C166 1000 SL
R111 3.3K
TH102 +7Ω
C106 25V 33μ
R112 2.2K
R113 8.2K
R114 2.2K
Q102 2SA1037K
R118 100K
C151 5
R142 1M
16V x10
C152 47P
C157 16V 1μ
C158 16V 1μ
TAN
S103
R136 47K
R137 47K
R138 47K
R139 47K
R140 47K
R134 47K
R131 47K
R141 47K
R121 47K
R1E6 47K
R1E7 47K
R1E8 47K
R1E9 47K
L105~L108, L111, L112
C121 820P

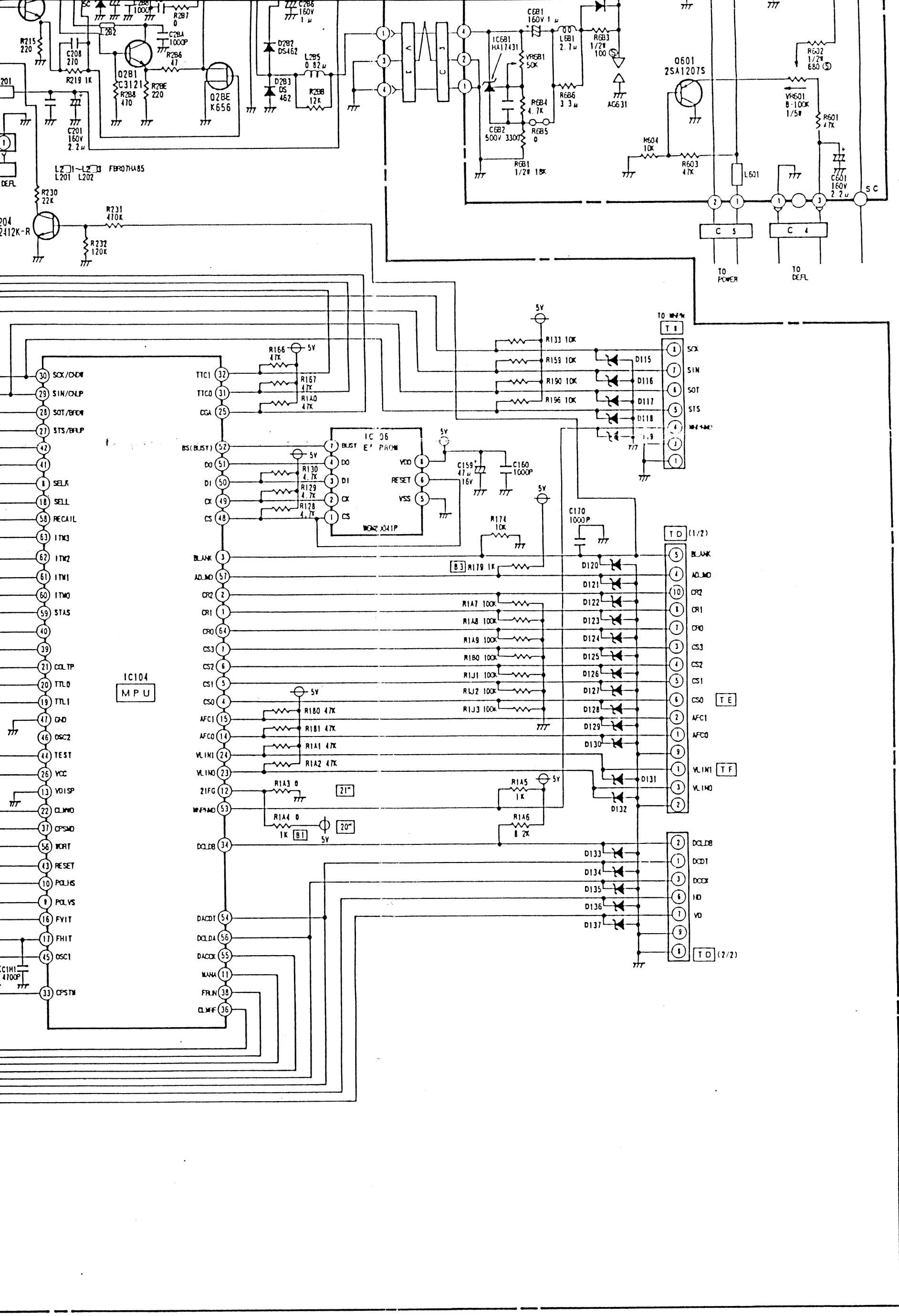

TO5
L1R4
R1RE 75
C1R6 16V 33μ
L1G4
R1GE 75
C1G6 16V 33μ
L1B4
R1BE 75
C1B6 16V 33μ
L1H3
R1H6 180
L1V3
R1V6 180
L1R2
L1R3
L1G3
L1B2
L1B3
L1□1~L1□3 FBR07HA85
R1H9 1K
R1V9 1K
C1VA 50V 1000P
R101 1K
R102 1K
R103 1K
R152 1K
R157 1K
R160 1K
D1R1 HZK11TRLLD
D1R2 HZK11TRLLD
D1G2 HZK11TRLLD
D1B1 HZK11TRLLD
D1B2 HZK11TRLLD
R1E0 1K
R1E1 1K
R1E2 1K
R1E3 1K
R1E4 1K
R1E5 1K
C1R3 SL1B
C1R4 SL1B
C1G3 SL1B
C1G4 SL1B
C1B3 SL1B
C1B4 SL1B
R136 47K
R137 47K
R134 47K
R139 47K
R140 47K
R134 47K
R131 47K
R141 47K
S103
R121 47K
R1E6 47K
R1E7 47K
R1E8 47K
R1E9 47K
L105~L108, L111, L112 FBR07HA850
D101~D113, D115~D127 HZK11TRLLD
(2/2)
L106
L107
L108
L110
L109
D101
D102
D103
D104
D105
C112 1000P
C111 1000P
C161 1000P
C104 16V 47μ
C105 16V 47μ
C162 1000P
5V
12V
TA
L105
C101 1000P
C177 16V 10μ
C172 1000
C173 16V 47μ
C165 1000 S L
C114 16V 22
C166 1000 S L
C113 16V 22
C106 25V 33μ
TH102 +7Ω
R111 3.3K
R112 2.2K
R113 8.2K
R114 2.2K
R115 3.9K
R116 3.9K
R118 100K
1C103 NJM2904M
Q103 2SC2412K -R
Q102 2SA1037K
C143 16V 33μ
C144 16V 33μ
R1H2 39K
R1H3 220
R1H4 39K
R1V2 39K
R1V3 220
R1V4 39K
Q1H1 2SK360
Q1V1 2SK360
C1H9 1000P
C1V9 1000P
C120 0.49
R1HB 680
R1HM 0
R1HN 82K
D1HB 1S2076A
D1HC 1S2076A
D1HD HZ3C3
C176 16V 47μ
R104 2.2K
L116
R1V7 330
R1V8 330
R109 22
Q114 A103
C122 16V 1μ
R185 22K
C124 33μ 16V
C164 1μ
L112
C151 5
R142 1M
C152 47P
C157 16V 1μ
C158 16V 1μ
R147 180
R146 180
R143 180
R110 560
R117 560
R119 560
R120 180
R122 180
R123 180
D1R5
R1R8 150
C1B2 25V 33μ
R1B6 100
R1B7
D1B3
D1B4
D1B5
R1B8 150
R1GA 75
R1G8 220
R1G6 100
R1G7
R1G8 150
D1G3
D1G4
D1G5
D1□3 ~D1□5 MA170FD /MA150FD
100 R1B6


T72
T71
IC105
STANDARD
CELL
5V
12V
L112
L202
S201
L111
L113 3.9μ
C203 25V 220μ
C204 1000
C164 1μ
C153 1000P
C151 51P
C152 47P
C157 16V 1μ
C158 16V 1μ
C171 1000P
C176 16V 47μ
C121 820P
C122 16V 1μ
C123 1000P
C124 33μ 16V
C127 16V 10μ
C142 0.1μ 50V
C178 0.1μ
C179 0.1μ
C180 0.1μ
C181 0.1μ
R132 180
R124 470
R125 470
R126 470
R127 470
R135 180
R162 180
R163 180
R164 180
R148 470
R1F 1K
R1F1 10K
R1F2 1K
R1F3 10K
R1F4 10K
R1F5 10K
R1F6 10K
R1F7 470
R132 180
R142 1M
R158 220
16MHZ X101
R144 1K
R145 10K
R171 1K
R1B4 47K
R1B5 47K
R1B6 47K
R1B7 47K
R161 47K
R175 0
R176 0
R178 470
R182 470
R168 47K
R106 8.2K-F
R107 4.7K-F
R108 1.8K
R172 6.8K
R173 3.3K
R109 22
R183 33K
R186 10K
R187 12K-F
R188 820-F
R184 10K
R185 22K
R189 3.6K-F
R191 100
R192 18K
R194 1K
R193 10K
R195 10K
R177 100
R197 12K-F
R198 560-F
R199 3.6K-F
R1V7 330
R1V8 330
D1R5
D1R8 150
D1B3
D1B4
D1B5
D1B8 150
D1G8 150
D1G3
D1G4
D1G5
D1□3 ~D1□5
MA170FD
/MA150FD
D106 D107 D108 D109 D110 D111 D112 D113
D140 HZK7BTR
D141 HZK3BTR
D1H0 HZ3G3
Q114 A1037
Q115 A1037
R146 180
R143 180
R110 560
R117 560
R119 560
R120 180
R122 180
R123 180
16V 1μ
16V 47μ
TAN
1000P
0.018μ
0.018μ
1000P
1000P
1000P


IC105
STANDARD CELL
Q1A2
Q1A6
Q1R3
Q1G3
Q1B3
Q1C2
Q1C6
Q1R4
Q1G4
Q1B4
Q1D2
Q1D6
Q1R5
Q1G5
Q1B5
Q107~Q111
2SC2412K
Q107
Q108
Q109
Q110
Q111
Q203
2SA1037
Q201
2SC2412K
Q1□2, 6 = 2SC2412K-R
Q1□3~5 = 2SC3735
T71
T72
S201
L111
L112
L113
L114
L115
L201
L202
D106
D107
D108
D109
D110
D111
D112
D113
D201
D202
D203
D2R1
D2G1
D2B1
MZ310
D1□3~D1□5
MA170FD
/MA150FD
5V
12V
16V 33μ ×3
C110 16V 47μ
C117 1000P
C118 1000P
C115 1000P
C119 1000P
C174 16V 47μ
C175 1200P
C205 50V 1μ
C206 1000
C203 25V 220μ
C204 1000
C156 1μ
C164 1μ
C153 1000P
C151 51P
C152 47P
C157 16V 1μ
C158 16V 1μ
C171 1000P
R2R9 0
R2G9 0
R2B9 0
R2R4 24K
R2G4 24K
R2B4 24K
R2R5 1000
R2G5 1000
R2B5 1000
R2R1 47
R2G1 47
R2B1 47
R2B3 15K
R2G3 15K
R2R3 15K
R212 10K
R221 15K
R222 10K
R213 6.8K
R224 8.2K
R223 22K
R207 8.2K
R208 470K
R209 100K
R205 10K-F
R226 47K
R108 8.2K-F
R107
R171 1K
R1B4 47K
R1B5 47K
R1B6 47K
R1B7 47K
R161 47K
R175 0
R176 0
R178 470
R182 470
R168 47K
R144 1K
R145 10K
R142 1M
16MHZ x101
R158 220
R132 180
R124 470
R125 470
R126 470
R127 470
R135 180
R162 180
R163 180
R164 180
R148 470
R153 1K
R154 10K
R155 10K
R156 10K
R157 470
R143 180
R110 560
R117 560
R119 560
R120 180
R122 180
R123 180
R1B8 150
R1G8 150
R1R8 150
R1D0 150
R1D2 150
R1D4 150
R1D6 150
R1D8 150
R1C8 100
C1R2 25V 33μ
C1G2 25V 33μ
C1B2 25V 33μ
C2B2 25V 47μ
C2G2 25V 47μ
C2R2 25V 47μ
C2B3 1000
C2G3 1000
C2R3 1000
L2B1
L2G1
L2R1
1SF RLAL
OTCH
OHCH
OCLMPH
OABDV
OAGDV
OARDV
OACNT
OABRT
ICLMCH
ICPMCH
IMORTH
OPESTH
OPMH
OPVH
OFVITL
OFHITH
OAMHZH
OBMHZH
ICP TMI
IDPH
IOPTRH
ISTRSTH
IRSTH
OVSBNH
IOVSH
IVSBIH
IVSBNH
IVSBNZH
IOGSH
OGSTNH
IGSTIH
IGSTMH
IGSTNH
IGSTZH
IDCODTH
IDCCKH
IDCLDH
OBANAH
IBFLH
IBCFLH
VSS
OTIL
VSS
ITIH
ITANAH
OTSH
VDD
VSS
VSS
IRSH
VSS
VDD
ITSH
IT2H
OSTILL
OCANAL
OCBNCL
STTL
SANA
SSNC
OTZL
LOSRTSL
IOPENTIH
IORUNCH
IWSDSH
IYSDSH
IOLOCH
OCLMFH
VSS
IRTH
IT2H
OUH
ITH
OXVH
ITVH
OXCOH
IVCOH
IOHSH
IHSBNH
IWSB
IW


IC201 M51387P
IC2R1 VPA05
IC2G1 VPA05
IC2B1 VPA05
IC104 MPU
IC 06 E² PROM
R-CUT-OFF
G-CUT-OFF
B-CUT-OFF
TO DEFL
L2□1~L2□3 FBR07HA85
L201 L202
Q203 2SA1037
Q201 2SC2412K
Q202 C2412K
Q204 C2412K-R
Q2R1 C3121
Q2R2 K656
Q2G1 K3121
Q2G2 K656
Q2B1 C3121
Q2BE K656
IC6R1 HA17431
IC6G1 HA17431
IC6B1 HA17431
SCK/CKDI
SIN/CKLP
SOT/BFDI
STS/BFLP
SELR
SELL
RECAIL
ITN3
ITN2
ITN1
ITN0
STAS
COLTP
TTL0
TTL1
GND
OSC2
TEST
VCC
VDISP
CLMN0
CPSM0
WORT
RESET
POLHS
TTC1
TTC0
CGA
BS(BUSY)
DO
DI
CK
CS
BLANK
ADJMD
CR2
CR1
CR0
CS3
CS2
CS1
CS0
AFC1
AFC0
VLIN1
VLIN0
21FG
DCLDB
21"
20"
B3
B1

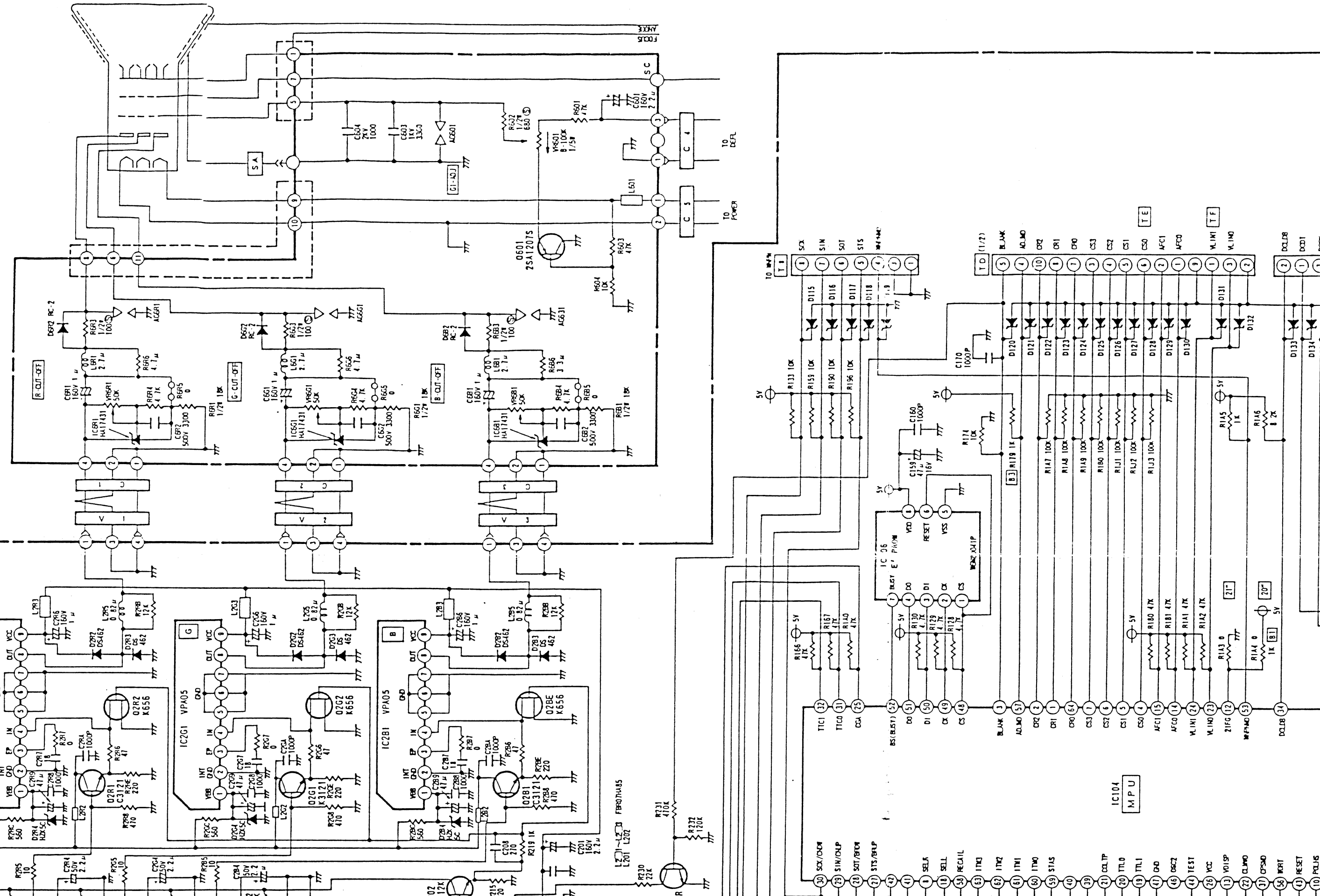

D203
S201
L201
L202
C203 25V 220μ
C204 1000
V 8
V 7
TO DEFL
L201~L203 FBR07HA85
L201 L202
C201 160V 2.2μ
R215 220
R218 5.6K
C208 270
R219 1K
Q2B1 C3121
R2B8 470
R2BE 220
Q2BE K656
R2B6 47
R2B7 0
C2B1 1000P
C2B2
D2B7 DS462
D2B3 DS 462
L2B5 0.82μ
R2B8 12K
C6B1 160V 1μ
L6B1 2.7μ
IC6B1 HA17431
VR6B1 50K
R6B4 4.7K
R6B5 0
R6B6 3.3μ
C6B2 500V 3300
R6B1 1/2W 18K
R230 22K
Q204 C2412K-R
R231 470K
R232 120K
5V
R133 10K
R159 10K
R190 10K
R196 10K
R166 47K
R167 47K
R1A0 47K
R130 4.7K
R129 4.7K
R128 4.7K
IC 06
E² PROM
C159 47μ 16V
C160 1000P
R174 10K
B3 R179 1K
R1A7 100K
R1A8 100K
R1A9 100K
R1B0 100K
R1J1 100K
R1J2 100K
R1J3 100K
R180 47K
R181 47K
R1A1 47K
R1A2 47K
R1A3 0
21"
R1A4 0
1K B1
20"
R1A5 1K
R1A6 8.2K
R171 1K
R184 47K
R185 47K
R186 47K
R187 47K
R161 47K
R175 0
R176 0
R178 470
R182 470
L113 3.9μ
R168 47K
L111
C158 1μ
C154 1000P
C101 0.01μ
C1V1 4700P
C1H1 4700P
C180 0.1μ
C181 0.1μ
R197 12K-F
R198 560-F
R199 3.6K-F
IC104
M P U
30 SCX/CKDI
29 SIN/CKLP
28 SOT/BFDI
27 STS/BFLP
42
41
8 SELR
18 SELL
58 RECAIL
63 ITM3
62 ITM2
61 ITM1
60 ITM0
59 STAS
40
39
21 COLTP
20 TTL0
19 TTL1
47 GND
46 OSC2
44 TEST
26 VCC
13 VDISP
22 CLMPO
37 CPSMO
56 WORT
43 RESET
10 POLHS
9 POLVS
16 FVIT
17 FHIT
45 OSC1
33 CPSTM
TTC1 32
TTC0 31
CGA 25
BS(BUSY) 52
DO 51
DI 50
CK 49
CS 48
BLANK 3
ADJMO 57
CR2 2
CR1 1
CR0 64
CS3 7
CS2 6
CS1 5
CS0 4
AFC1 15
AFC0 14
VLIN1 24
VLIN0 23
21FG 12
DCLDB 34
DACDT 54
DCLDA 56
DACCK 55
FRUN 38
CLMPF 36
BUSY 7
DO 4
DI 3
CK 2
CS 1
VDD 8
RESET 6
VSS 5

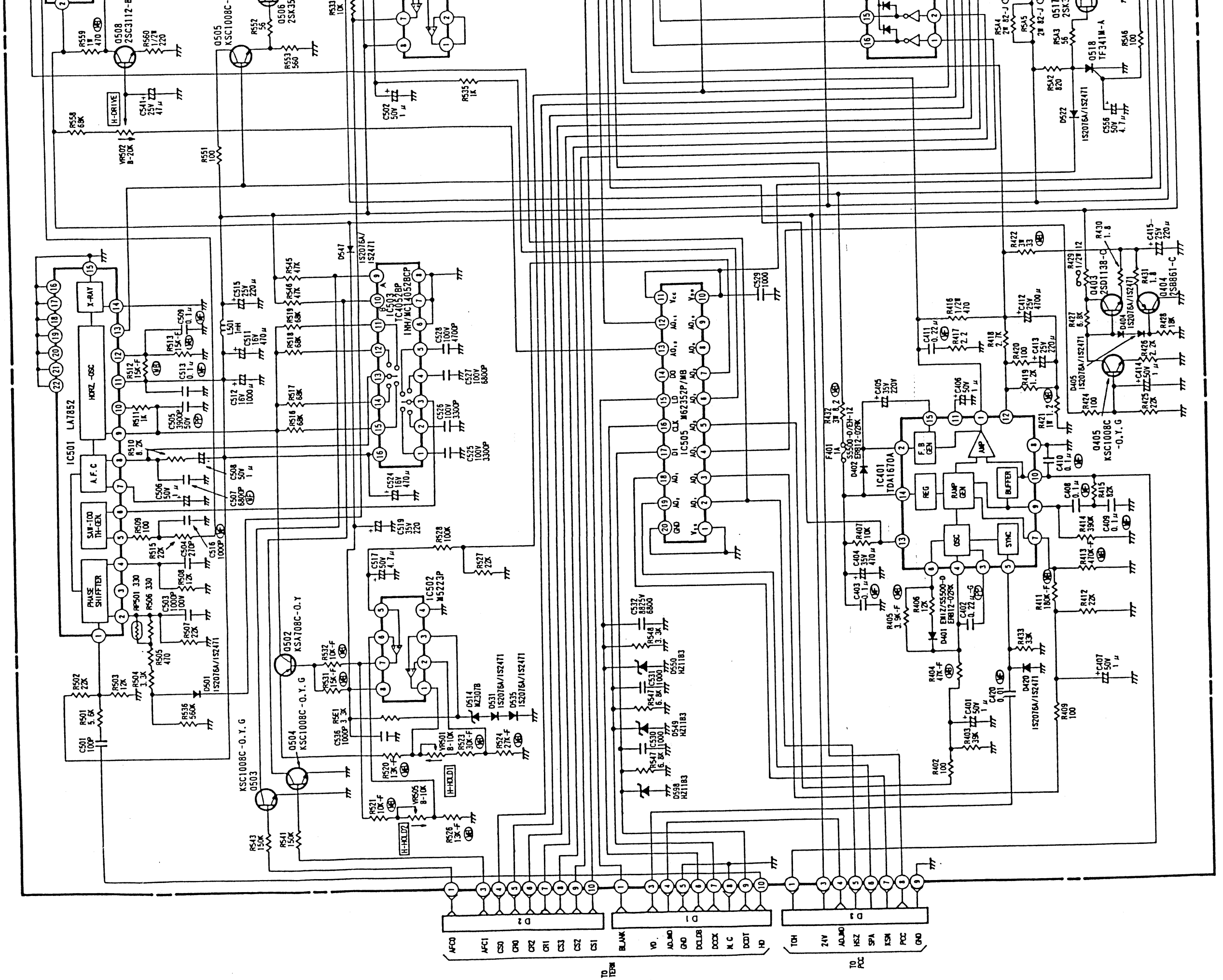


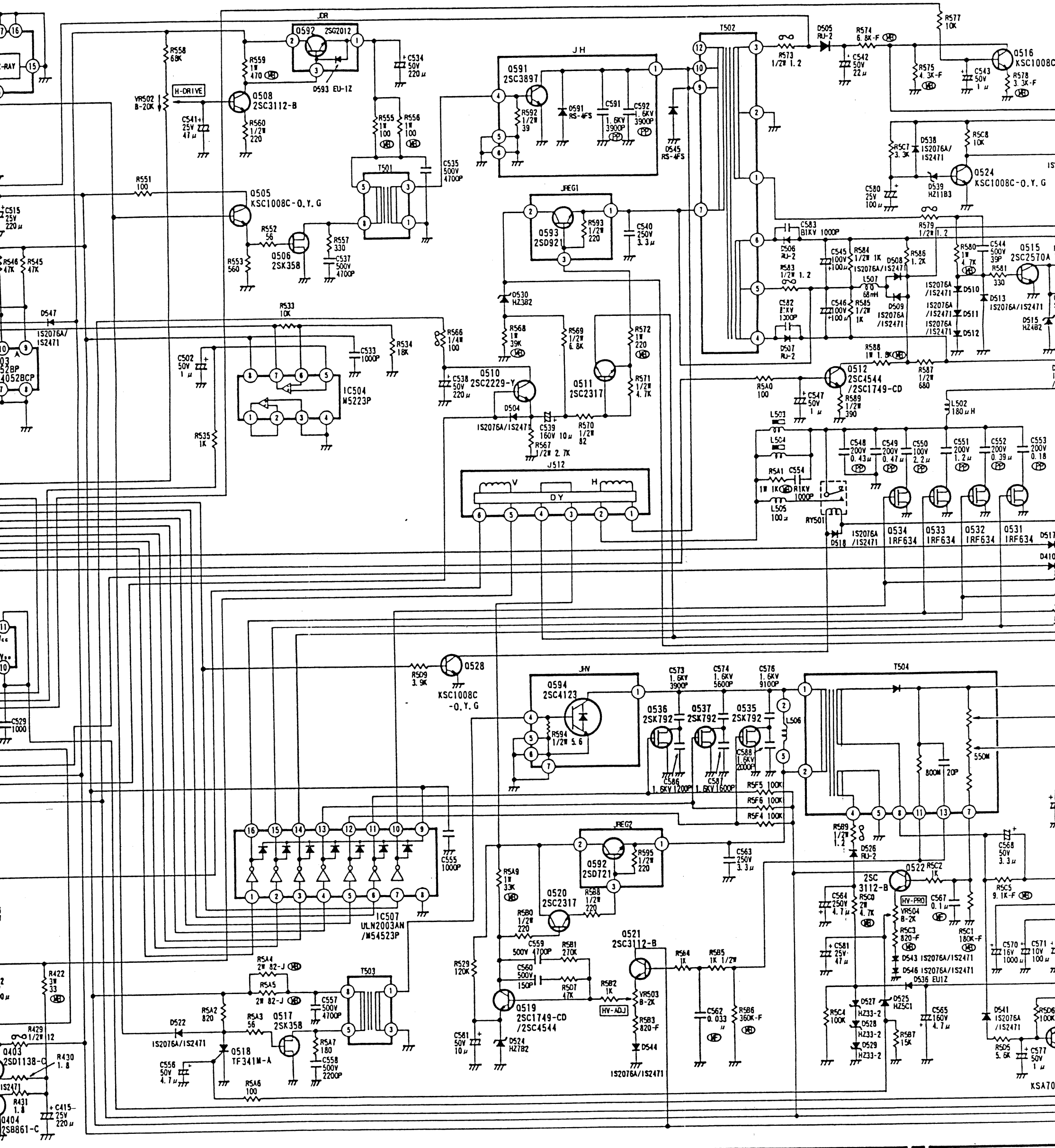
MODEL:HC3925

TERMINAL-VIDEO CIRCUIT

4/


R-CUT-OFF
G-CUT-OFF
B-CUT-OFF
IC2R1 VPA05
IC2G1 VPA05
IC2B1 VPA05
IC104
M P U
IC 06
E² PROM
TO DEFL
TO POWER
TO MAIN
5V
SCK
SIN
SOT
SIS
BLANK
ADJMD
CR2
CR1
CR0
CS3
CS2
CS1
CS0
AFC1
AFC0
VLIN1
VLIN0
DCLDB
DCD1
SCK/DCKM
SIN/DLP
SOT/BRDM
SIS/BRLP
SELA
SELL
RECVIL
INT2
INT1
INT0
SIAS
COLTP
TTL0
TTL1
GND
OSC2
TEST
VCC
VOLSP
CLAMPO
CPSAO
RORT
RESET
POLIS


IC501 LA7852
X-RAY
HORZ. OSC
A.F.C
SAW-TOO TH-GEN
PHASE SHIFTER
IC503 TC4052BP INH/MC14052BCP
IC505 M62352P/MB
IC401 TDA1670A
F.B GEN
REG
RAMP GEN
BUFFER
AMP
OSC
SYNC
IC502 M5223P
Q502 KSA708C-O.Y
Q504 KSC1008C-O.Y.G
Q503 KSC1008C-O.Y.G
Q505 KSC1008C-O.Y.G
Q508 2SC3112-B
Q518 TF341M-A
Q403 2SD1138-C
Q404 2SB861-C
H-DRIVE
VR502 B-20K
VR501 B-10K
VR505 B-10K
H-HOLD1
H-HOLD2
TO TERM
TO PCC
AFC0
AFC1
CS0
GND
CK2
CK1
CS3
CS2
CS1
BLANK
VD
ADJVD
GND
DCLOB
DCCK
N.C
DCDT
HD
TCH
24V
ADJVD
HSZ
SPA
KSN
PCC
GND


JDR
Q592 2SG2012
D593 EU-1Z
R558 68K
VR502 B-20K
H-DRIVE
C541+ 25V 47μ
Q508 2SC3112-B
R560 1/2W 220
R559 1W 470
C534 50V 220μ
R555 1W 100
R556 1W 100
T501
C535 500V 4700P
R551 100
Q505 KSC1008C-O.Y.G
R552 56
R553 560
Q506 2SK358
R557 330
C537 500V 4700P
JH
Q591 2SC3897
R592 1/2W 39
D591 RS-4FS
C591 1.6KV 3900P
C592 1.6KV 3900P
D545 RS-4FS
JHEG1
Q593 2SD921
R593 1/2W 220
C540 250V 3.3μ
T502
D505 RU-2
R573 1/2W 1.2
R574 6.8K-F
C542 50V 22μ
R575 4.3K-F
R577 10K
C543 50V 1μ
Q516 KSC1008C
R578 3.3K-F
R5C7 3.3K
D538 IS2076A/IS2471
R5C8 10K
Q524 KSC1008C-O.Y.G
D539 HZ11B3
C580 25V 100μ
C583 B1KV 1000P
R579 1/2W 1.2
D506 RU-2
C545 100V +100μ
R584 1/2W 1K
IS2076A/IS2471
D508
R586 1.2K
R583 1/2W 1.2
L507 68mH
C582 B1KV 1200P
C546 100V +100μ
R585 1/2W 1K
D509 IS2076A /IS2471
R580 1W 4.7K
C544 500V 39P
R581 330
Q515 2SC2570A
IS2076A /IS2471 D510
D513 IS2076A/IS2471
D511
D512
D515 HZ48Z
D507 RU-2
R588 1W 1.8K
R587 1/2W 680
Q512 2SC4544 /2SC1749-CD
R5A0 100
C547 50V 1μ
R589 1/2W 390
L502 180μH
L503
L504
R5A1 1W 1K
C554 B1KV 1000P
L505 100μ
RY501
C548 200V 0.43μ
C549 200V 0.47μ
C550 100V 2.2μ
C551 200V 1.2μ
C552 200V 0.39μ
C553 200V 0.18
D518 IS2076A /IS2471
Q534 IRF634
Q533 IRF634
Q532 IRF634
Q531 IRF634
D517
D410
R547 47K
R546 47K
C515 25V 220μ
D547
IS2076A/ IS2471
C502 50V 1μ
R533 10K
C533 1000P
R534 18K
IC504 M5223P
R535 1K
R566 1/4W 100
C538 50V 220μ
Q510 2SC2229-Y
R568 1W 39K
R569 1/2W 6.8K
Q511 2SC2317
R572 1W 220
R571 1/2W 4.7K
D504 IS2076A/IS2471
C539 160V 10μ
R567 1/2W 2.7K
R570 1/2W 82
D530 HZ3B2
J512
V
H
DY
C529 1000
Q528 KSC1008C -O.Y.G
R5D9 3.9K
JHV
Q594 2SC4123
R594 1/2W 5.6
C573 1.6KV 3900P
C574 1.6KV 5600P
C576 1.6KV 9100P
Q536 2SK792
Q537 2SK792
Q535 2SK792
L506
C586 1.6KV 1200P
C587 1.6KV 1600P
C588 1.6KV 2000P
R5F5 100K
R5F6 100K
R5F4 100K
T504
550M
800M 20P
R589 1/2W 1.2
D526 RU-2
C568 50V 3.3μ
C555 1000P
JREG2
Q592 2SD721
R595 1/2W 220
C563 250V 3.3μ
R5A9 1W 33K
Q520 2SC2317
R588 1/2W 220
R580 1/2W 220
C559 500V 4700P
R581 270K
C560 500V 150P
R507 47K
R582 1K
Q521 2SC3112-B
R564 1K
R585 1K 1/2W
C562 0.033μ
R586 360K-F
R529 120K
C581 50V 10μ
D524 HZ7B2
Q519 2SC1749-CD /2SC4544
VR503 B-2K
HV-ADJ
R583 820-F
D544
IS2076A/IS2471
Q522 2SC 3112-B
R5C2 1K
R5C0 2W 4.7K
HV-PRO
VR504 B-2K
C567 0.1μ
R5C5 9.1K-F
C564 250V 4.7μ
R5C3 820-F
R5C1 180K-F
C581 25V 47μ
D543 IS2076A/IS2471
D546 IS2076A/IS2471
D536 EU1Z
R5C4 100K
D527 HZ33-2
D528 HZ33-2
D529 HZ33-2
D525 HZ5C1
R5B7 15K
C565 160V 4.7μ
D541 IS2076A /IS2471
R5D6 100K
R5D5 5.6K
C577 50V 1μ
C570 16V 1000μ
C571 10V 100μ
IC507 ULN2003AN /M54523P
R5A4 2W 82-J
R5A5 2W 82-J
T503
R5A2 820
R5A3 56
Q517 2SK358
C557 500V 4700P
D522 IS2076A/IS2471
Q518 TF341M-A
R5A7 180
C558 500V 2200P
C556 50V 4.7μ
R5A6 100
R422 3W 33
R429 1/2W 12
Q403 2SD1138-C
R430 1.8
R431 1.8
Q404 2SB861-C
C415 25V 220μ
KSA70

MODEL:HC3925

DEFLECTION CIRCUIT

TIMING DATA

TIMING NO.	DOT IN t_{HD}	t_H	t_{HS}	t_{Hb}	t_{Hd}	t_V	t_{VS}	t_{Vb}	t_{Vd}	POLARITY		REMARKS
										H Sync.	V Sync.	
1	640	63.50	4.50	8.95	44.5	16.637	0.190	2.159	12.7	P	P	CGA
2	640	45.76	4.62	2.06	39.30	16.84	0.595	0.137	16.016	P	N	EGA (CH.)
3	640	46.40	4.95	2.40	39.50	17.00	0.60	0.103	16.30	P	N	EGA (GRA.)
4	720	31.78	3.80	1.96	25.42	14.269	0.064	1.875	11.127	P	N	VGA350
5	720	31.780	3.800	1.900	25.480	14.269	0.064	1.081	12.712	N	P	VGA400
6	640	31.780	3.800	1.960	25.420	16.685	0.064	1.017	15.254	N	N	VGA480
7	1024	28.150	3.920	1.25	22.80	11.485	0.112	0.563	10.810	P	P	8514A
8	640	28.560	2.120	3.320	31.18	14.994	0.086	1.114	13.709	C	—	MAC II